User Manual

Tektronix

VX4286
32-Channel Analog/Digital Input Module

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This document applies for firmware version 1.00
and above.

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EC Declaration of Conformity

We

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declare under sole responsibility that the

VX4286 and all options

meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:

EN 55011 Class A Radiated and Conducted Emissions

EN 50081-1 Emissions:

EN 60555-2 AC Power Line Harmonic Emissions

EN 50082-1 Immunity:

IEC 801-2 Electrostatic Discharge Immunity
IEC 801-3 RF Electromagnetic Field Immunity
IEC 801-4 Electrical Fast Transient/Burst Immunity
IEC 801-5 Power Line Surge Immunity

To ensure compliance with EMC requirements this module must be installed in a mainframe which has backplane shields installed which comply with Rule B.7.45 of the VXIbus Specification.

RSTX [A_1],[A_2], ... [A_n] resets all EXCEPT the specified portions of the module to its power-up state. (3 - 75)

SET [A],[B],[C] programs the time used for time tagging. (3 - 76)

STB [A] specifies when to latch into the digital input latches the data present on the digital input lines. (3 - 78)

SYNC [A] specifies which signal synchronizes the time tag counter. (3 - 80)

SYNC? returns whether or not a SYNC signal has come in. (3 - 81)

SYNCOFF disables the SYNC signal. (3 - 82)

TRG [TRIGDEF] programs the voltage level threshold and logic sense or trigger condition of each channel. (3 - 83)

TRGH [TRIGDEF] programs the voltage level threshold and logic sense or trigger condition of each channel, within the ±50V range. (3 - 86)

TRGL [TRIGDEF] programs the voltage level threshold and logic sense or trigger condition of each channel, within the ±10V range. (3 - 87)

VOLT? [L],[B] returns DC voltage of the input channel. (3 - 89)

VOLTALL? [L],[CHANNEL STRING] takes a voltage measurement on all channels simultaneously. (3 - 91)

VOLTALLH? [L],[CHANNEL STRING] takes a voltage measurement within the ±50V range on all channels simultaneously. (3 - 93)

VOLTALLL? [L],[CHANNEL STRING] takes a voltage measurement within the ±10V range on all channels simultaneously. (3 - 94)

VOLTAVE specifies that only the average voltage should be returned from one of the VOLT commands. (3 - 95)

VOLTFULL specifies that the maximum, minimum, and average voltages should be returned form one of the VOLT commands. (3 - 96)

VOLTH? [L],[B] returns the dc voltage of the specified input channel within the ±50V range. (3 - 97)

VOLTL? [L],[B] returns the dc voltage of the specified input channel within the ±10V range. (3 - 98)

VOLTNEXT? optional. Used when a command is required before readback. (3 - 99)

VX4286 MODULE QUICK REFERENCE GUIDE

Numbers in parentheses refer to the page(s) in the Operating Manual.

SETUP

Be sure all switches are correctly set. (p. 1 - 3)
Follow Installation guidelines. (p. 2 - 1)

The default condition of the VX4286 Module after the completion of power-up self test is listed in the Specifications sub-section.

LEDs

When lit, the LEDs indicate the following:

Power	power supplies functioning
Failed	module failure
ERR	an error has been found in self test or programming
MSG	module is processing a VMEbus cycle
ARM	in Analog mode, whenever this module is armed to monitor inputs
ANA/DIG	on in Analog or Combination Analog/Digital mode; off in Digital mode

Front Panel Display

In Analog mode, the front panel displays which channel is on the "wrong" side of its threshold (realtime or latched data). If multiple channels are on the "wrong" side, the channel with the highest priority will be displayed.

In Digital mode, the states of 16 bits of input in hexadecimal are displayed (realtime or latched data).

SYSTEM COMMANDS

These low-level commands are typically sent by the module's commander, transparent to the user, except for the Read STB command. See page 3 - 5 for details.

Clear	Asynchronous Mode Control	
Begin Normal Operation	Abort Normal Operation	
Read Protocol	End Normal Operation	
Read Status	Control Event	
Set Lock	Read Protocol Error	
Clear Lock	Byte Available	
Read Interrupters	Byte Request	
Read Interrupt Line	Control Response	Trigger

MODULE COMMANDS

A number of commands have two forms, a short and longer syntax. Either form can be used. All commands end with a terminator (LF or ;). For a complete description of command protocol and syntax, see page (3 - 7).

ABREV [A] returns the BUF OVFLW and NO ENTRIES messages in abbreviated form when reading the event buffer. (3 - 13)

ANADIG [A] selects combination Analog/Digital mode. (3 - 14)

ANALOG selects the Analog mode. (3 - 15)

APER [A] specifies aperture time for VOLT? command. (3 - 16)

ARM [A] programs when to ARM the module to begin monitoring the inputs. (3 - 17)

ARM? returns whether or not the module is armed. (3 - 19)

BUF? returns whether the Event buffer is full or empty. (3 - 20)

CAL [A],[B] used to calibrate this module. (3 - 21)

CAL? returns a message specifying whether or not all channels have been calibrated. (3 - 23)

CLR clears all comparator status latches. (3 - 24)

DATA? [R],[Q] in Digital mode, returns the values of the digital inputs or digital input latches. In Analog mode, returns the Event buffer, which contains all channels detected on the "wrong" side of their respective thresholds. (3 - 25)

DATAANA? [R],[Q] returns information about which channels were detected on the "wrong" side of their respective thresholds. (3 - 26)

DATADIG? [R],[Q] returns the values of the digital inputs or digital input latches. (3 - 27)

DBENB [N_1], ...[N_x] enables or disables debounce of the selected inputs. (3 - 28)

DBTIME [A],[B] specifies debounce time for channels using debounce circuitry. (3 - 29)

DIGITAL selects the Digital mode. (3 - 30)

DINT [A],[B] disables generation of the VXIbus Request True interrupts. (3 - 31)

DISPANA [A],[B] defines how data is to be presented on the front panel display during Analog mode. (3 - 32)

DISPBYTE [N],[M] defines which bytes of data are displayed on the front panel display in Digital mode. (3 - 34)

DISPDIG [A] defines how data is presented on the display in Digital mode. (3 - 35)

DISPENB [A] defines the set of channels that may be displayed in Analog mode. (3 - 36)

DISPPRI [CHANNEL STRING] defines the priority of the channels for the display in Analog mode. (3 - 37)

ENB [CHANNEL STRING] enables any bit and TTL output in Digital mode. (3 - 38)

EQU [F],[E],[EQUATION] defines the condition that will cause a channel to be recorded and a Request True interrupt to be generated. It also specifies which channels are enabled or disabled during Analog mode. (3 - 39)

EQURST resets the equation period. (3 - 42)

EQUPOL [A] sets the polarity of the EQU OUT signal. (3 - 43)

ERR? instructs this module to return its error status next time input is requested from the module. (3 - 44)

FCAL [A] routes calibration signal to front panel for calibrating 5 ppm crystal oscillator (Option 01 only). (3 - 48)

FLIPCONT [CHANNEL STRING] continually reverses the trigger sense (polarity) of a particular channel. (3 - 49)

FLIPDIS [CHANNEL STRING] disables the flip capability of a particular channel. (3 - 50)

FMTANA [A],[B],[C],[D],[E] defines the format of the Event buffer, which is returned by the DATA? command when in Analog mode. (3 - 51)

FMTDIG [A],[B] defines the format of the data returned by the DATA? command in Digital mode. (3 - 60)

HYST [A] turns programmable hysteresis on and off. (3 - 62)

INT [A] enables generation of the VXIbus Request True interrupts. (3 - 63)

INT? returns the bottom four bits on the VXI status register, which denotes the state of the VXIbus Request True interrupt. (3 - 64)

INT2? identical to the INT? command except it resets the interrupt condition (and bits 1 and 0) every time it is executed. (3 - 65)

IST initiates a self test. (3 - 66)

NAME [C],[N] gives a name to a channel for display on the front panel. (3 - 68)

OUTPUT [A] enables TTL outputs. (3 - 69)

REENB [F],[E],[Q],[CHANNEL STRING] re-enables selected channels when in Analog mode. (3 - 70)

REV? returns the revision level of the onboard microprocessor firmware. (3 - 72)

RST [A_1],[A_2], ... [A_n] resets all or part of the module to the power-up state. (3 - 73)

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

Injury Precautions

Avoid Electric Overload. To avoid electric shock or fire hazard, do not apply a voltage to a terminal that is outside the range specified for that terminal.

Avoid Electric Shock. To avoid injury or loss of life, do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Do Not Operate Without Covers. To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Use Proper Fuse. To avoid fire hazard, use only the fuse type and rating specified for this product.

Do Not Operate in Wet/Damp Conditions. To avoid electric shock, do not operate this product in wet or damp conditions.

Do Not Operate in an Explosive Atmosphere. To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

Product Damage Precautions

Provide Proper Ventilation. To prevent product overheating, provide proper ventilation.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

DANGER
High Voltage

Protective Ground
(Earth) Terminal

ATTENTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

VX4286
32-Channel
Analog/Digital Input Module

Section 1
General Information and Specifications

Introduction

The VX4286 32-Channel Analog/Digital Input Module is a single width, C size printed circuit board assembly for use in a C size or larger mainframe conforming to the VXIbus Specification. The thirty-two inputs of the VX4286 Module can be configured under program control to function either as thirty-two digital inputs (Digital mode), as thirty-two comparator inputs with time tagging (Analog mode), or as sixteen channels of each (combination Analog/Digital mode).

In either mode, all input channels have individually programmable threshold voltages and can be programmed to active high or active low logic. Two logic threshold ranges are provided: ±10V with an accuracy of 40 mV and resolution of 5 mV, or ±50V with an accuracy of 100 mV and resolution of 25 mV. Each channel may be programmed to use either range or it may be instructed to autorange, selecting the most sensitive range suitable for a specified threshold voltage. The VX4286 also includes facilities for input signal conditioning modules, such as pullups for open collector outputs, A/C detection, or user-designed input circuitry.

The front panel display shows which channel, if any, is on the "wrong" side of its threshold. The display can represent real time data, or latest event data, with user specified priority taken into account. All channels can be programmed to have user definable names for displaying.

Thirty-two TTL output lines are provided on the VX4286 that reflect the state of the comparator status latch of each input comparator. Another TTL output provides an external signal when any comparator status latch becomes set. It can also be programmed to not become active until some predefined AND/OR combination of inputs has occurred.

A voltmeter capability will read back the DC voltage level on any channel. A set of commands controls the voltage information received, including maximum, minimum, and average of maximum and minimum voltage levels, the range to be used, and whether specified channels or all channels are to be measured.

Analog Mode

In the Analog mode, this module's function is to detect whether or not a channel is ever on the "wrong" side of a programmably defined threshold, where the "wrong" side can be defined as either above or below the threshold. Complex AND/OR equations can be set up to define upon what set of conditions the interrupt occurs. The VX4286 continuously monitors each analog input line for an input voltage level which is greater than, or less than, the programmed threshold voltage. When a voltage of the proper value is detected, the "true" condition is captured in a latch, time tagged, and stored on the VX4286.

In Analog mode, information on any channel detected on the "wrong" side of its threshold is stored in the Event buffer, which can hold up to 1414 entries. An entry is recorded each time an enabled channel or group of channels is noticed on the "wrong" side of their respective thresholds. Each entry includes the time that the channel(s) were detected, the polarity of each channel (above or below the threshold) at this time, and whether or not the channel(s) were just enabled.

Normally, a VXI Request True interrupt is then generated (in IEEE 488 systems, the Request True interrupt generates an SRQ on the IEEE 488 bus), but interrupts can also be programmed to be generated on complex AND/OR conditions of multiple channels. The VX4286 can optionally be polled. The system controller can interrogate the VX4286 at any time to determine which channel was detected on the "wrong" side of its threshold, and the time it happened. The monitoring feature can be enabled under program control or by an external Arm command.

The format selection for the returned data can be based on the application. For example, the data may be formatted to include such information as: relative or absolute time tag; channel information (bit encoded or by channel number); channel number; and an individual ("as-it-happened") report or cumulative ("everything-that-happened") report.

Additional features available in Analog mode include debounce and pulse detection. Debounce control is ideally suited for monitoring contact closures and can be enabled or disabled under program control in groups of four inputs. Debounce time can be programmed from 1/10 millisecond to 6 seconds. The FLIP command, by providing the ability to automatically switch trigger sense each time a transition occurs, facilitates the detection and characterization of pulses. The TTL output lines provide a positive pulse with a pulse width equal to the trigger uncertainty time (typically 100 microseconds) whenever a channel is on the "wrong" side of the defined threshold. When memory is full, the TTL output lines will be constant high.

Digital Mode

In the Digital mode, the module acts as a digital input module with programmable voltage thresholds. A threshold is defined for each bit, and whether a 1 or a 0 defines being above the threshold. The data on the input can be read at any time, returned in hex or binary format. An external user supplied strobe may also be enabled to latch data in before it is read.

In Digital mode, input data is sampled at the time an input request is made by the system controller, or when an external strobe pulse is received. The front panel display shows the states of sixteen of the thirty-two bits, as selected by the user under program control. The display can represent real time or last latched data. The TTL output lines function as hardware level shifters, converting the programmed input logic levels to TTL output logic levels on a continuous basis.

BITE (Built-In Test Equipment)

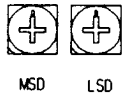
Self test for this module verifies that all input thresholds are tested to within 5% of their required accuracy. It also tests the correct operation of the on-board RAM, non-volatile RAM, slave microprocessor, and field programmable gate array.

Controls And Indicators

The following controls and indicators are provided to select and display the functions of the VX4286 Module's operating environment. See Figures 1 and 2 for their physical locations.

Switches

Logical Address Switches



Each function module in a VXIbus System must be assigned a unique logical address, from 1 to 255 decimal. The base VMEbus address of the VX4286 is set to a value between 1 and FFh (255d) by two hexadecimal rotary switches. Align the desired switch position with the arrow on the module shield.

The actual physical address of the VX4286 Module is on a 64 byte boundary. If the switch representing the most significant digit (MSD) of the logical address is set to position X and the switch representing the least significant digit (LSD) of the logical address is set to position Y, then the base physical address of the VX4286 will be [(64d * XYh) + 49152d]. For example:

L.A.	MSD	LSD	Base Physical Addr. (d)
Ah	0	A	(64*10)+49152 = 49792d
15h	1	5	(64*21)+49152 = 50496d

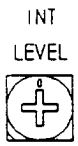
where: L.A. = Logical Address
MSD = Most Significant Digit
LSD = Least Significant Digit

IEEE-488 Address

Using the VX4286 Module in an IEEE-488 environment requires knowing the module's IEEE-488 address in order to program it. Different manufacturers of IEEE-488 interface devices may have different algorithms for equating a logical address with an IEEE-488 address.

If the VX4286 is being used in a MATE system, VXIbus logical addresses are converted to IEEE-488 addresses using the algorithm specified in the MATE IAC standard (MATE-STD-IAC).

VMEbus Interrupt Level Select Switch



Each function module in a VXIbus System can generate an interrupt on the VMEbus to request service from the interrupt handler located on its commander (for example, the VX4520 Slot 0 Device/Resource Manager in a VX7401 IEEE-488 Interface System). The VMEbus interrupt level on which the VX4286 Module generates interrupts is set by a BCD rotary switch. Align the desired switch position with the arrow on the module shield.

Valid Interrupt Level Select switch settings are 1 through 7, with setting 1 equivalent to level 1, etc. The level chosen should be the same as the level set on the VX4286's interrupt handler, typically the module's commander. Setting the switch to 0 or 8 will disable the module's interrupts. Switch setting 9 should not be used. When using the VX4286 in a VX7401 System, set the interrupt level to the same level chosen on the VX4520.

Interrupts are used by the module to return VXIbus Protocol Events to the module's commander. Refer to the Operation section for information on interrupts. The VXIbus Protocol Events supported by the module are listed in the Specifications section.

Halt Switch

This two-position slide switch selects the response of the VX4286 Module when the Reset bit in the module's VXIbus Control register is set. Control of the Reset bit depends on the capabilities of the VX4240's commander.

If the Halt switch is in the ON position, the VX4286 Module is reset to its power-up state and all programmed module parameters are reset to their default values.

If the Halt switch is in the OFF position, the module will ignore the Reset bit and no action will take place.

Note that the module is not in strict compliance with the VXIbus Specification when the Halt switch is OFF.

LEDs

Power LED

This green LED is normally lit and is extinguished if the +5V or ±24V power supplies fail, if the +5V or ±24V fuses blow, or if the embedded ±15V, -7.5V, or positive reference power supplies derived on-board the VX4286 fail.

Failed LED

This normally off red LED is lit whenever SYSFAIL* is asserted, indicating a module failure. Module failures include failure to correctly complete an interface self test, loss of a power rail, or failure of the module's central processor. The LED will remain lit

while the error condition exists, independent of the setting of the Sysfail Inhibit bit in the VXIbus Control register.

NOTE: If the module loses any of its power voltages, the Failed LED will be lit and SYSFAIL* asserted. A module power failure is indicated when the module's Power LED is extinguished.

MSG LED
This green LED is normally off. When lit it indicates that the module is processing a VMEbus cycle. The LED is controlled by circuitry that appears to stretch the length of the VMEbus cycle. For example, a 200 nanosecond cycle will light the LED for approximately 0.2 seconds. The LED will remain lit if the module is being constantly addressed.

Error LED
This red LED indicates that an error was found while attempting to execute a command sent to the module. This includes out of range and syntax errors. The error that caused this LED to light can be determined by the ERR? (error query) command. The LED is cleared when the ERR? command is executed and all errors have been read.

ARM LED
This green LED is on in Analog mode whenever this module is armed to monitor inputs.

ANA/DIG LED
This green LED is on when in Analog or Combination Analog/Digital mode. It is off when in Digital mode.

Front Panel Display
The meaning of the information displayed on the front panel depends upon whether the module is in Digital or Analog mode.

If in Analog mode, the front panel displays which channel, if any, is on the "wrong" side of its threshold. You may specify either realtime or latched data. If multiple channels are on the "wrong" side, the channel with the highest priority (as specified by the DISPANA PRIORITY command) will be displayed. Each channel is given its own name for display purposes. Upon power-up or reset, channel 0 has the name CH00, channel 1, CH01 and so forth. Any channels can be programmably renamed at any time.

In Digital mode, the states of 16 bits of input in hexadecimal is displayed. Which bits are displayed can be programmed in groups of eight bits via the DISPDIG command. Either realtime or latched data may be selected.

Front Panel Signal Connections
There are two 50 pin D connectors (32 channel inputs, with 32 TTL output lines, daughter board common voltage signal, and clock synchronization signal). There are also two BNC connectors (Arm/Strobe input, EQU OUT output).

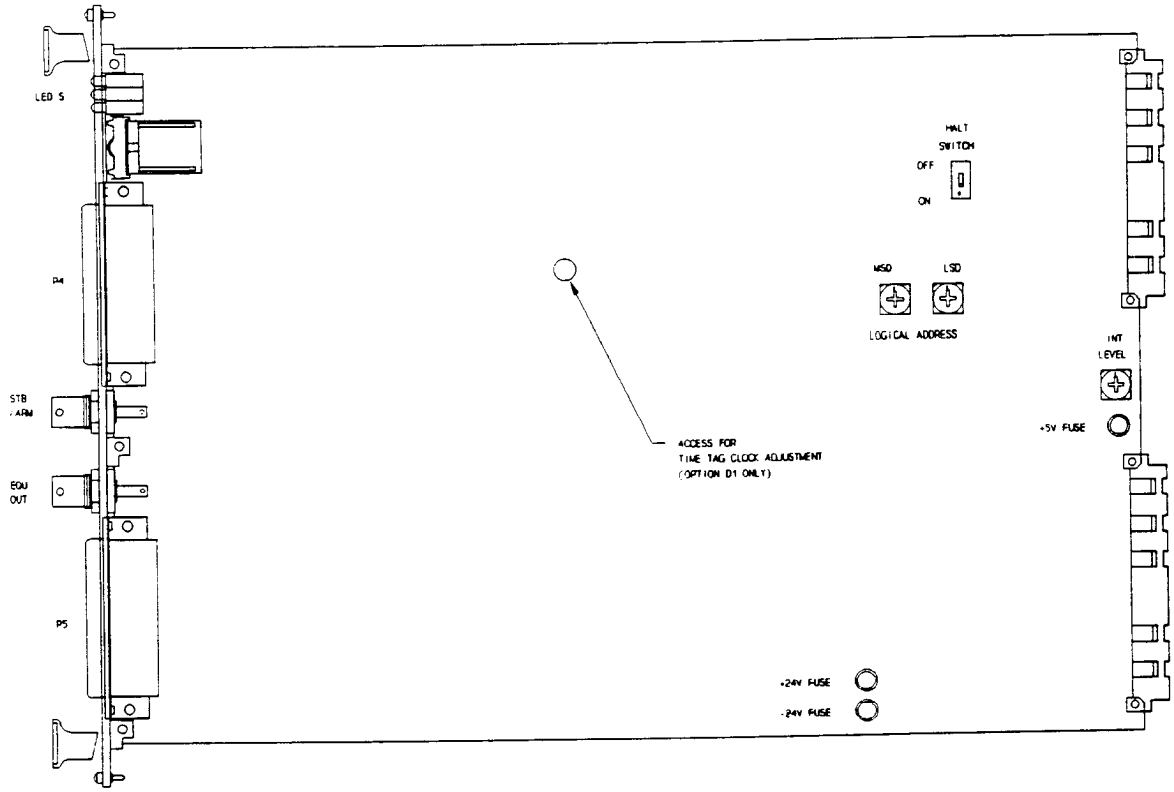


Figure 1: VX4286 Controls and Indicators

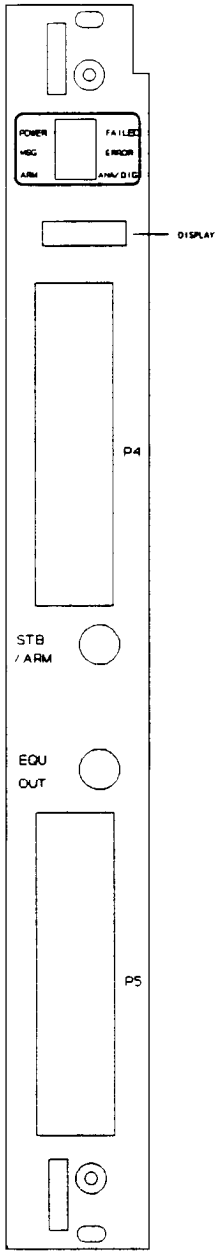


Figure 2: VX4286 Front Panel

Specifications

Digital Input Mode

Inputs:	32 bits.
Logic Threshold:	Each bit separately programmable, ±50V in 25mV steps or ±10V in 5mV steps. Range is programmable.
Logic Sense:	Programmable: active high or active low.
Strobe Input:	Logic sense: programmable, positive/negative going transition or ignored. Logic Threshold: TTL level compatible.
Arm/Strobe Input (Digital Mode):	In Digital mode, this input can be enabled to act as the strobe input. This signal strobes all digital input latches simultaneously. Programmably enabled/disabled. Minimum pulse width: 50 ns. Polarity: Programmable.
TTLTRG* (Digital Mode):	Compliant with VXIbus defined Synchronous Trigger Protocol. In Digital mode or Combination Analog/Digital mode, any one of these inputs can be enabled to act as the strobe input or to synchronize the time tag counter. Individually programmable enable/disable. Minimum pulse width: 10 ns. Polarity: Active low per VXIbus defined Synchronous Trigger Protocol.

Analog Comparator Mode

Inputs:	32 bipolar analog input channels.
Logic Threshold:	Programmable by channel ±50V in 25mV steps or ±10V in 5mV steps. Range is programmable.
Trigger Condition:	Programmable by channel, greater or less than voltage threshold. Condition may be disabled, on a by-channel basis.
Trigger Programmability:	May program an interrupt and the EQU OUT signal to occur on any positive logic AND/OR combination of threshold occurrences on any of the 32 channels. Programmed via sum-of-products Boolean equation.
Hysteresis, TTL Outputs:	This is the hysteresis which exists on the inputs with respect to the TTL Outputs. 15 mV.

Hysteresis, Recording Into Event buffer:

This hysteresis defines a voltage range such that an input signal will not be recorded until it exceeds the programmed voltage plus half this value, and will not be recorded again until it goes below the programmed voltage minus half this value. This implies the Flip bit is set on this channel (FLIPCONT command) and that programmable hysteresis has been activated (HYST command). For further details, see TRG command.

Programmable in steps of 5mV (±10V range), or 25mV (±50V range), over the entire range.

Default hysteresis (if not specified in command) is 15mV (both ranges).

Minimum Pulse Width:

Input Step size	Overdrive	Minimum Pulse Width
(both ranges)		
100 mV	50 mV	3.0 µsecs
	500 mV	0.5 µsecs
	5 V	0.2 µsecs
1V	50 mV	8 µsecs
	500 mV	2 µsecs
	5 V	1 µsecs
5V	50 mV	9 µsecs
	500 mV	3 µsecs
	5 V	2 µsecs
(±50V range only)		
25V	250 mV	9 µsecs
	2.5 V	3 µsecs
	25 V	2 µsecs

Time Tag Clock Accuracy:

50 ppm (5 ppm clock available as an option).

Time Tag Uncertainty:

This is the maximum time interval between when an event occurs and when its time tag is recorded. See the Time Tag Uncertainty sub-section for details.

EQU OUT Output:

Pulses when a defined AND/OR combination of threshold occurrences has occurred.

Polarity: Programmable.

Pulse width: 2.4 µsec.

Delay from when the event occurs and pulse occurs is equal to the time tag uncertainty.

Arm/Strobe Input (Analog Mode):

In Analog mode, this input acts as the Arm input. It can be programmed to be active (do not begin monitoring inputs until the ARM pulse) or disabled (module is continually monitoring inputs).

Minimum pulse width: 50 ns.

Polarity: Programmable.

TTLTRG*
(Analog Mode): Compliant with VXIbus defined Synchronous Trigger Protocol. In Analog mode (but not in Combination Analog/Digital mode), any one of these inputs can be enabled to act as the arm input or to synchronize the time tag counter. In Combination Analog/Digital mode, these inputs cannot be used for the arm function, but may be used as the strobe function.

Minimum pulse width: 10 ns.
Polarity: Active low per VXIbus defined Synchronous Trigger Protocol.

Common Specifications

Overall Accuracy: 40 mV on ±10V range, 100 mV on ±50V range at 25° C.

Temperature Coefficient: 60 ppm/ degree C.

Calibration Cycle: 12 months.

Monitonicity: Guaranteed within either range.

Maximum Input: ±120V rms, 150V DC.

Input Impedance: 98K ohm (±10V range).
52K ohm (±50V range).

Debounce Counters: Two. Each group of four channels can be selectively enabled/ disabled. Channels 0-7 and 16-23 operate with debounce counter 1. Channels 8-15 and 24-31 operate with debounce counter 2.

Debounce Delay: This is the time delay that the input voltage may toggle before it is captured. Can be enabled or disabled in groups of four inputs. When enabled, programmable from 1/10 milliseconds to 6.5535 secs, in units of tenths of milliseconds.

Volt Meter Reading: 30 mV accuracy with a 2.5 mV resolution on the ±10 volt range; 100 mV accuracy with a 12.5 mV resolution on the ±50 volt range.

Programmed By: ASCII characters.

Power Up Conditions: When power is applied, the module goes to the following known states:

General
Power LED: lit.
Mode: Analog mode.
Threshold level: 1.4V.
Range: ±10 volt range.
Trigger sense: Greater than threshold level (>).
Comparator status latches: cleared.

TTL Outputs: tri-stated.
Error buffer: cleared.
Error LED: off.
Readback type: error buffer.
Interrupts: disabled.
Aperture time (for VOLT? command): 10 milliseconds.

Associated with Analog Mode
Module unarmed.
Inputs when in Analog mode: disabled.
EQU OUT signal polarity: active low.
Current time: zeroed.
Event buffer: cleared.
Analog readback format: returned by individual channel number, by event, relative time tag in seconds.
Channel names: CH<channel number> where <channel number> is a two digit number.
Analog display mode: real time.
Analog channel priority: 0 highest, 31 lowest.
Comparator status latches: cleared.
Flip bits: cleared (both sets).
Debounce counter time: 1/10 of a second.
Debounce enable: all channels disabled.
Source of Counter Synchronization Pulse: front panel P4
Programmable hysteresis: off.

Associated with Digital Mode
Inputs when in Digital mode: enabled.
External Strobe: Disabled, strobe on readback of digital data.
Digital readback format: ASCII hex, from digital input latches.
Digital display mode: real time.
Digital display byte order: 1,0, left to right.

TTL Output Lines:

Current output available per channel: 15 mA source, 24 mA sink.
Logic sense: active high.
Number of outputs: 32.
Function: Analog Mode - High if corresponding comparator status latch is set.
Digital Mode - High if corresponding input bit is true.

Power Requirements:

All required dc power is provided by the Power Supply in the VXIbus mainframe.

Voltage:

+5 Volt Supply: 4.75 V dc to 5.25 V dc.
+24 Volt Supply: +23.5 V dc to +24.5 V dc.
-24 Volt Supply: -23.5 V dc to -24.5 V dc.

Current (Peak Module, I_{PM}):	5 volt supply: 2.0 A +24 volt supply: 130 mA -24 volt supply: 120 mA +12 volt supply: 0 A -12 volt supply: 0 A -5.2 volt supply: 0 A -2.0 volt supply: 0 A
Replacement Fuses:	+24V: Littelfuse P/N 273002 -24V: Littelfuse P/N 273002 +5V: Littelfuse P/N 273005
Cooling:	Provided by fans in the VX1400 Mainframe. The module will have a temperature rise of < 10°C with 0.9 liters/sec per slot of air and a pressure drop of 0.16 mm of H_2O.
Temperature:	0°C to +50°C, operating. -40°C to +85°C, storage.
Humidity:	Less than 95% R.H. non-condensing, 0°C to +30°C. Less than 75% R.H. non-condensing, +31°C to +40°C. Less than 45% R.H. non-condensing, +41°C to +50°C.
VXIbus Radiated Emissions:	Complies with VXIbus Specification.
VXIbus Conducted Emissions:	Complies with VXIbus Specification.
Module Envelope Dimensions:	VXI C size. 262 mm x 353 mm x 30.5 mm (10.3 in x 13.9 in x 1.2 in)
Dimensions, Shipping:	When ordered with a Tek/CDS mainframe, the module is installed and secured in one of the instrument module slots (slots 1 - 12). When ordered alone, shipping dimensions are: 406 mm x 305 mm x 102 mm. (16 in x 12 in x 4 in).
Weight:	1.44 kg. (3.2 lb).
Weight, Shipping:	When ordered with a Tek/CDS mainframe, the module is installed and secured in one of the instrument module slots (slots 1 - 12). When ordered alone, shipping weight is: 1.89 kg. (4.2 lb).
Mounting Position:	Any orientation.

Mounting Location:	Installs in an instrument module slot (slots 1-12) of a C or D size VXIbus mainframe. (Refer to D size mainframe manual for information on required adapters.)
Front Panel Signal Connections:	Two 50 pin male D connectors (32 channel inputs, 32 TTL output lines, daughter board common voltage signal, clock synchronization signal). Two BNC (Arm/Strobe input, EQU OUT output).
Recommended Cable or Connectors:	VX1733 Cable or VX1780S Hooded Connector.
Equipment Supplied:	1 - VX4286 Module.
Software Revision:	V2.2

Section 2
Preparation For Use

Installation Requirements And Cautions

The VX4286 Module is a C size VXIbus instrument module and therefore may be installed in any C or D size VXIbus mainframe slot other than slot 0. If the module is being installed in a D size mainframe, consult the operating manual for the mainframe to determine how to install the module in that particular mainframe. Setting the module's Logical Address switch defines the module's programming address. Refer to the Controls and Indicators subsection for information on selecting and setting the module's logical address. To avoid confusion, it is recommended that the slot number and the logical address be the same.

Tools Required

The following tools are required for proper installation:

Slotted screwdriver set.

CAUTION

Note that there are two printed ejector handles on the card. To avoid installing the card incorrectly, make sure the ejector marked "VX4286" is at the top.

In order to maintain proper mainframe cooling, unused mainframe slots must be covered with the blank front panels supplied with the mainframe.

Based on the number of instrument modules ordered with the mainframe, blank front panels are supplied to cover all unused slots. Additional VXIbus C size single-slot and C size double-slot blank front panels can be ordered from your Tektronix supplier.

CAUTION

Verify that the mainframe is able to provide adequate cooling and power with this module installed. Refer to the mainframe Operating Manual for instructions.

If the VX4286 is used in a VX1X Series Mainframe, all VX4286 cooling requirements will be met.

CAUTION

If the VX4286 Module is inserted in a slot with any empty slots to the left of the module, the VME daisy-chain jumpers must be installed on the backplane in order for the VX4286 Module to operate properly. Check the manual of the mainframe being used for jumpering instructions.

If a VX1400 Mainframe is being used, the jumper points may be reached through the front of the mainframe. There are five (5) jumpers that must be installed for each empty slot. The five jumpers are the pins to the left of the empty slot.

Installation Procedure

CAUTION

The VX4286 Module is a piece of electronic equipment and therefore has some susceptibility to electrostatic damage (ESD). ESD precautions must be taken whenever the module is handled.

1) Record the Revision Level, Serial Number (located on the label on the top shield of the VX4286), and switch settings on the Installation Checklist. Only qualified personnel should perform this operation.

2) Verify that the switches are switched to the correct values. The Halt switch should be in the ON position unless it is desired to not allow the resource manager to reset this module.

   Note that with either Halt switch position, a "hard" reset will occur at power-on and when SYSRST* is set true on the VXIbus backplane. If the Module's commander is a VX4520 Slot 0 Device/Resource Manager, SYSRST* will be set true whenever the Reset switch on the front panel of the VX4520 is depressed. Also note that when the Halt switch is in the OFF position, the operation of this module is not VXIbus compatible.

3) Make sure power is off in the mainframe.

4) The module can now be inserted into one of the instrument slots of the mainframe.

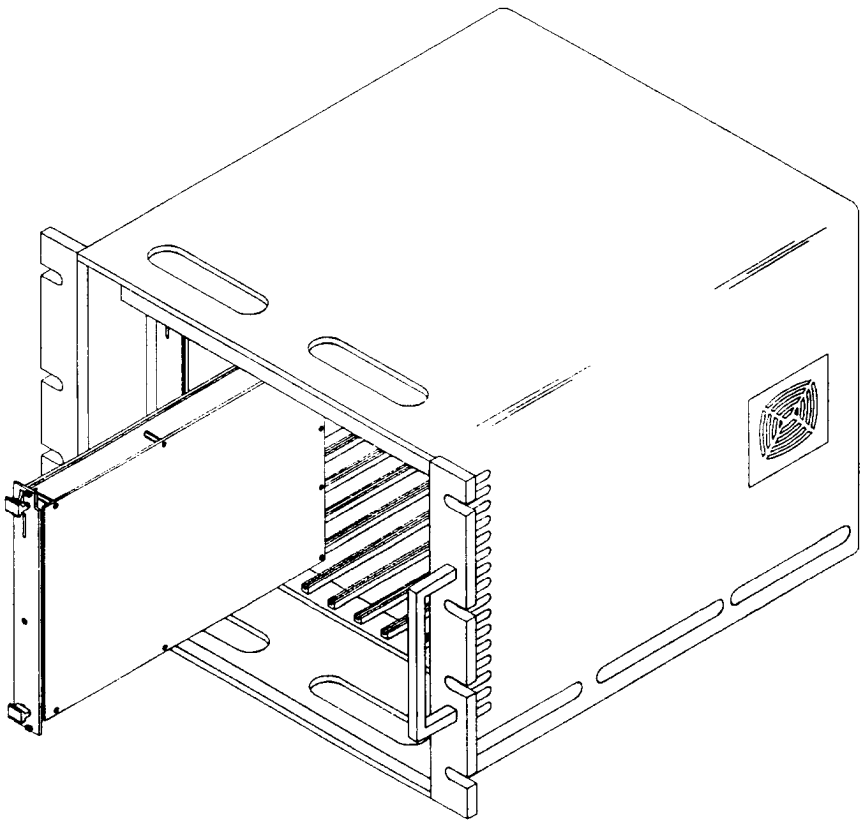


Figure 3: Module Installation

5) Cable Installation -

Use the appropriate cable to interface between the module I/O connector and the Unit Under Test (UUT). If the module is being installed in a Tek/CDS VX1400 or VX1401 Mainframe, route the cable from the front panel of the module down through the cable tray at the bottom of the mainframe and out the rear of the mainframe.

The mainframe is interfaced to the system controller using a standard IEEE-488 cable to connect the IEEE-488 connector on the rear panel of the VX1400 Mainframe to the IEEE-488 interface connector at the system controller.

Installation Checklist

Installation parameters will vary depending on the mainframe being used. Be sure to consult the mainframe Operating Manual before installing and operating the module.

Revision Level: _____

Serial No.: _____

Mainframe Slot Number: _____

Switch Settings:

VXIbus Logical Address Switch: _____

Interrupt Level Switch: _____

Halt Switch: _____

Cable / Hooded Connector Installed:

Cable: _____

Hooded Connector: _____

Performed by: _____ Date: _____

Section 3
Operation

Overview

The VX4286 Module is programmed by ASCII characters issued from the system controller to the VX4286 Module via the module's VXIbus commander and the VXIbus mainframe backplane. The module is a VXIbus Message Based Device and communicates using the VXIbus Word Serial Protocol. Refer to the manual for the VXIbus device that will be the VX4286 Module's commander for details on the operation of that device.

The VX4286 Module has two operational modes, the Digital and the Analog mode.

In the Digital mode, the module acts as a digital input module with programmable voltage thresholds. A threshold is defined for each bit, and whether a 1 or a 0 is defined for values above the threshold. The data on the input can be read at any time, returned in hex or binary format. An external user-supplied strobe may also be enabled to latch data in before it is read.

The normal setup and operation of the Digital mode is as follows:

1) Set module to Digital mode (DIGITAL command).

2) Program all thresholds (TRG, TRGH, or TRGL command).

3) Set up readback format (FMTDIG command).

4) Enable TTL outputs if they are being used (OUTPUT command).

5) Set up whether the external strobe is enabled or disabled and, if enabled, its polarity (STB command).

6) Enable the proper channels (default condition is all channels enabled) (ENB command).

7) Read data back at any time (DATA? command).

In the Analog mode, this module's function is to detect whether or not a channel is ever on the "wrong" side of a programmably defined threshold. When this occurs, an interrupt is generated, and information can be read back about the time the signal was detected on the "wrong" side of the threshold, and the channels detected. The "wrong" side can be defined as either above or below the threshold. Complex AND/OR equations can be set up to define upon what set of conditions the interrupt occurs.

The normal setup and operation of the Analog mode is as follows:

1) Set module to Analog mode (ANALOG command).

2) Program all thresholds (TRG, TRGH or TRGL command).

3) Set up proper readback format (FMTANA)

4) Enable the proper channels and define the set of conditions on which an interrupt and the EQU OUT signal should be generated. (If enabled; see the EQU command.)

5) If using interrupts, enable interrupt generation (INT EQU)

6) Arm this module or enable an external ARM signal to arm this module (ARM command).

7) Wait for an interrupt (SRQ on IEEE-488 systems) or poll the module with the BUF?, INT?, or INT2? command.

8) When an interrupt occurs (or the correct bit returned by the INT? or INT2? command is set or a non-zero response is returned by the BUF? command), read back which channel(s) were on the "wrong" side of their thresholds, and record or print out this data (DATA? or DATA? R command). If interrupts were used, they should be cleared by performing the Read STB command (which corresponds to a Serial Poll on IEEE-488 systems).

9) If the DATA? R command was used, the channel(s) that are subsequently read back will automatically be re-enabled to have information on them recorded again. If they are still on the "wrong" side of the threshold, they will cause another interrupt.

   Go back to step 7.

10) If the DATA? command was used in step 8, the channel(s) that are subsequently read back are not re-enabled and will never cause another interrupt until a REENB or EQU command is sent, UNLESS a channel has the Flip Continuous bit set, in which case it has stayed enabled.

    Go back to step 7, OR send a REENB command, to re-enable the channels that have already caused an interrupt to interrupt again.

Event Buffer

In Analog mode, information on any channel detected on the "wrong" side of its threshold is stored in the Event buffer, which can hold up to 1414 entries. An entry is recorded each time an enabled channel or group of channels is noticed on the "wrong" side of their respective thresholds. Each entry includes the time that the channel(s) were detected, the polarity of each channel (above or below the threshold) at this time, and whether or not the channel(s) were just enabled. For channels with the Flip

Continuous bit not set, there is usually either no entry or one entry corresponding to the channel in the Event buffer. For channels with the Flip Continuous bit set, there may be a number of entries. Should this buffer become filled, it will be re-enabled again to take in another entry with every entry read out.

When an enabled channel is detected on the "wrong" side of its threshold, the channel disables itself until it is either read with a DATA? R command or the REENB or EQU command is sent. However, if the channel has its Flip Continuous bit set, it remains enabled until disabled by a EQU command with its channel no longer specified.

The Event buffer contents are returned with the DATA? or DATA? R command in Analog mode, and may be returned one entry at a time or all entries at once (cumulatively). The format of the returned data is defined by the FMTANA command. The returned format for a normal entry is always in the form:

[OC][TIME TAG]:<SP>[CHANNEL DATA]<CR><LF>

where [TIME TAG]:<SP> and [OC] will only be returned if specified in the FMTANA command. <CR><LF> is optionally returned when binary data is specified. [OC], [TIME TAG], and [CHANNEL DATA] formats are fully explained in the FMTANA command description.

[TIME TAG] may be either fixed or unfixed format. In fixed format it will always have the following character length, padded with leading blanks.

Length	Time Tag Format	
12	SEC,MSEC,TMSEC	seconds,milliseconds,tenths of milliseconds
18	DHMS	days/hours/minutes/seconds
22	DATE	date

In unfixed format, there is no padding with leading blanks. Examples of response data with the time tag are given in the FMTANA command.

[OC], if selected to be returned, is a single character, and specifies whether a buffer overflow condition has occurred when the reading data cumulatively option has been chosen. If the overflow condition has occurred, [OC] will be the character V. Otherwise it will be a space character (20 hex). Examples of response data with the [OC] character included are given in the FMTANA command.

There are two special condition messages that may be returned.

NO ENTRIES<CR><LF> is returned if there are no remaining collected entries.

BUF OVFLW: [MESSAGE]<CR><LF> is returned if the input buffer has overflowed when reading data by individual events. If reading data cumulatively, this message is not returned; the [OC] character may be used to detect an overflow condition. (The choice of reading data by individual events or cumulatively is selected in the FMTANA command.) There are only two situations that can cause a buffer overflow:

1) if a channel has its Flip Continuous bit set, and is continually transitioning about the threshold to the point where it fills up the input buffer, or,

2) if the F (force) option of EQU or REENB command is being continually sent, without reading data back.

If absolute time tag is specified, [MESSAGE] takes the form:

DATA LOST FROM [TIME1] TO [TIME2]

where [TIME1] represents the time when data was first lost, and [TIME2] represents the time when space in the buffer became available again (due to an entry being read out). [TIME1] and [TIME2] are in the time tag format specified by the FMTANA command (including whether or not [TIME1] and [TIME2] are fixed field).

If relative time tag is specified, [MESSAGE] takes the form:

[TIME1] [UNITS] OF DATA LOST AT REL TIME [TIME2]

where [TIME1] represents the time period during which data was lost, and [TIME2] represents the time relative to the previous entry, when an entry was lost. [TIME1] and [TIME2] are in the time tag format specified by the FMTANA command (including whether or not [TIME1] and [TIME2] are fixed format). If the specified time tag format is seconds, tenths of milliseconds, or milliseconds, [UNITS] will take on the value SECS, TENTHS OF MSECS, or MSECS, respectively. [UNITS] will not be part of the message for any other time tag format.

If no time tag is specified, [MESSAGE] takes the form:

[TIME1] [UNITS] OF DATA LOST

where [TIME1] and [UNITS] are the same as defined above.

Time Tag Uncertainty

The time tag uncertainty is the maximum time interval between when an event occurs and when its time tag is recorded.

An event is defined as the detection of an enabled channel on the "wrong" side of its threshold. An event is either a first or second event, depending on the interval between it and the previous event.

First Event: any event separated from a previous event by more than T μsecs (where T is Tt, Tf, Ta, or Tfa as listed under Second Event). The time tag uncertainty of the first event is: ≤ 100 μsec.

Second Event: any event occurring within T μsec after another event. The value of T depends on whether or not the Flip Continuous bit (FLIPCONT command) of a particular

channel is set, whether programmable hysteresis is enabled (HYST command), and whether AND/ORing is enabled (EQU command):

Tt: Flip bit not set
Tf: Flip bit set
Ta: Flip bit not set, AND/ORing enabled
Tfa: Flip bit set, AND/ORing enabled

	Prog. Hysteresis OFF	Prog. Hysteresis ON
Tt	≤ 400 μsec	≤ 400 μsec
Tf	≤ 400 μsec	≤ 1200 μsec
Ta	≤ 350 + (N*25) μsec*	≤ 350 + (N*25) μsec *
Tfa	≤ 350 + (N*25) μsec*	≤ 1200 + (N*25) μsec*

* rounded to the nearest 100 microseconds.

where N is the number of AND terms in the Boolean equation if AND/ORing is enabled. For example, for

EQU 0 to 31	N = 0
EQU 0 + 3 + 7	N = 0
EQU 0*3*4+7	N = 1
EQU 0*3*4+5*6+7*8	N = 3

Examples:

A command is sent to assert EQU OUT signal if chan 0 or chan 3 or chan 31 occur.
Applicable time spec: Tt

A command is sent to assert EQU OUT signal if chan 0 or chan 3 or both chan 31 AND 29 occur.
Applicable time spec: Ta (N = 1)

This is the same as the first example, with the Flip bit enabled. The Flip bit enables automatic switching of trigger sense each time an event occurs.
Applicable time spec: Tf

This is the same as the second example, with the Flip bit enabled.
Applicable time spec: Tfa (N = 1)

Power-up

The VX4286 Module will complete its self test and be ready for programming five seconds after power-up. The VXIbus Resource Manager may add an additional one or two second delay. The Power LED will be on, and all other LEDs off. The MSG LED will blink during the power-up sequence as the VXIbus Resource Manager addresses all modules in the mainframe. The default condition of the module after power-up is described in the SYSFAIL, Self Test and Initialization subsection.

System Commands

These low-level commands are typically sent by the module's commander, transparent to the user of the module. An exception is the Read STB command, which is sent whenever a Serial Poll on an IEEE-488 system is performed. Most commanders or Slot 0 devices have specific ASCII commands which will cause them to send one of these low-level commands to a specified instrument. Refer to the Operating Manual of the commander or Slot 0 device for information on these commands.

Command	Effect
Clear	The module clears its VXIbus interface and any pending commands. Current module operations are unaffected.
Begin Normal Operation	The module will begin operation per VXI Specification.
Read Protocol	The module will return its protocol to its commander.
Read STB	The module will return its VXI Status byte to its commander.
Set Lock	Set the LOCKED* bit of the Response register.
Clear Lock	Clears the LOCKED* bit of the Response register.
Read Interrupters	Returns the value FFF9, indicating there is one interrupter on this module.
Read Interrupt Line	Returns the interrupt line per VXI Specification.
Asynchronous Mode Control	Returns information that events are being sent as interrupts per VXI Specification.
Abort Normal Operation	Causes this device to cease normal operation per VXI Specification.
End Normal Operation	Causes this device to cease normal operation per VXI Specification.
Control Event	Used by a commander to selectively enable the generation of events by a servant.
Read Protocol Error	Returns the module's most recent error code, which includes multiple query errors, unsupported commands, and DOR violations.
Byte Available	Transfers module commands to this module.
Byte Request	Requests data be returned form the module.

Control Response Returns information indicating response interrupts are not supported.

Trigger This module will accept the Trigger command, although no part of this instrument will be affected by it.

Module Commands

A summary of the VX4286 Module's commands is listed following the syntax description. This is followed by detailed descriptions of each of the commands. A sample BASIC program using these commands is given in the Programming Examples section.

Command Syntax

Command protocol and syntax for the VX4286 Module are as follows:

1) Each command consists of a single line of any number of characters. Parameters may not be "wrapped around" (continued on the next line). Every command must end with a line feed <LF> or semi-colon (;) terminator. The terminator may be omitted from any command if the End bit (which corresponds to the EOI signal in IEEE-488 systems) is set on the last character of the command. Carriage-returns <CR> are optional before line feeds or semicolons.

2) If a character is not enclosed by brackets, that character itself is sent, otherwise:

   [ ] encloses the symbol for the actual argument to be sent. These argument symbols are defined under each command heading.

   < > indicates a binary value; ie: <0Ah> is a line feed.

   <CR> indicates a carriage return.

   <LF> indicates a line feed.

   <SP> indicates a space character.

   <TM> terminator: indicates a line feed or a semicolon.

3) Any character may be sent in either upper or lower case form.

4) Any of the following white space characters:

   00 hex
   01 hex through 08 hex
   09 hex (TAB character)
   0B hex through 19 hex (including carriage return)
   20 hex (SPACE character)

are allowed in any of the following places:

- before any comma, semicolon, or <LF>.
- after any comma.
- in place of any SPACE character listed on the syntax line in the command descriptions.

Any number of white space characters may be used together.

5) The white space between a command and its first parameter is optional. That is, both STB S and STBS are valid formats.

6) All numeric values, except numbers specifying channels, may be given in integer, floating point, or scientific notation. Numbers specifying channels must be given as integers.

A number of commands are given in two forms, a short and longer syntax. Either form can be used. For example, a DATA?<CR><LF> is equivalent to a D?<CR><LF> command.

Any command may be given in either the Digital or Analog mode, although some commands will only take effect in one mode or the other. For instance, the FMTANA (format of analog readback data) may be given in Digital mode, but it will not take effect until Analog mode is entered. Which mode the command applies to is given under 'Mode' in the command description.

Response Syntax

All responses end with a <CR><LF>, except where specified. The End bit is asserted with the <LF>. In the examples given in the command descriptions, the responses from the VX4286 are shown underlined.

Summary

Detailed descriptions of each command (in alphabetical order) are given following the summary.

ABREV [A]	returns the BUF OVFLW and NO ENTRIES messages in abbreviated form when reading the Event buffer.
ANADIG [A]	selects combination Analog/Digital mode.
ANALOG	selects the Analog mode.
APER [A]	specifies aperture time for VOLT? command.
ARM [A]	programs when to ARM the module to begin monitoring the inputs.
ARM?	returns whether or not the module is armed.
BUF?	returns whether the Event buffer is full or empty.
CAL [A],[B]	used to calibrate this module.
CAL?	returns a message specifying whether or not all channels have been calibrated.
CLR	clears all comparator status latches in Analog mode.
DATA? [R],[Q]	in Digital mode, returns the values of the digital inputs or digital input latches. In Analog mode, returns the Event buffer, which contains all channels detected on the "wrong" side of their respective thresholds.
DATAANA? [R],[Q]	returns the Event buffer.
DATADIG? [R],[Q]	returns the values of the digital inputs or digital input latches.
DBENB [N_1], ...[N_x]	enables or disables debounce of the selected inputs.
DBTIME [A],[B]	specifies debounce time for channels using debounce circuitry.
DIGITAL	selects the Digital mode.
DINT [A],[B]	disables generation of the VXIbus Request True interrupts.
DISPANA [A],[B]	defines how the data is to be presented on the front panel display during Analog mode.
DISPBYTE [N],[M]	

DISPDIG [A] defines how the data is to be presented on the front panel display during Digital mode.

DISPENB [A] defines the set of channels that may be displayed.

DISPPRI [CHANNEL STRING]
defines the priority of the channels for the display in Analog mode.

ENB [CHANNEL STRING]
used to enable any bit and corresponding TTL output in Digital mode.

EQU [F],[E],[EQUATION]
defines the condition that will cause a channel to be recorded and a Request True interrupt to be generated. It also specifies which channels are enabled or disabled during Analog mode.

EQURST resets the equation period.

EQUPOL [A] sets the polarity of the EQU OUT signal.

ERR? instructs this module to return its error status next time input is requested from the module.

FCAL [A] routes calibration signal to front panel for calibrating 5 ppm crystal oscillator (VX4286 Option 01 only).

FLIPCONT [CHANNEL STRING]
continually reverses the trigger sense (polarity) of a particular channel.

FLIPDIS [CHANNEL STRING]
disables the flip capability of a particular channel.

FMTANA [A],[B],[C],[D],[E]
defines the format of the Event buffer, which is returned by the DATA? command when in Analog mode.

FMTDIG [A],[B] defines the format of the data returned by the DATA? command in Digital mode.

HYST [A] turns programmable hysteresis on and off.

INT [A] enables generation of the VXIbus Request True interrupts.

INT? returns the bottom four bits of the VXI status register, which defines the state of a VXIbus Request True interrupt.

INT [A] enables generation of the VXIbus Request True interrupts.

INT? returns the bottom four bits of the VXI status register, which defines the state of a VXIbus Request True interrupt.

INT2? identical to the INT? command except it resets the interrupt condition (and bits 1 and 0 of the status byte) every time it is executed.

IST initiates a self test.

NAME [C],[N] gives a name to a channel to be displayed on the front panel.

OUTPUT [A] enables TTL Outputs.

REENB [F],[E],[Q],[CHANNEL STRING]
re-enables selected channels when in Analog mode.

REV? returns the revision level of the onboard microprocessor firmware.

RST $[A_1]$,$[A_2]$, ... $[A_n]$
resets the module or portions of the module to the power-up state.

RSTX $[A_1]$,$[A_2]$, ... $[A_n]$
resets all EXCEPT the specified portions of the module to its power-up state.

SET [A],[B],[C] programs the time used for time tagging.

STB [A] specifies when to latch into the digital input latches the data present on the digital input lines.

SYNC [A] specifies which signal synchronizes the time tag counter.

SYNC? returns whether or not a SYNC signal has come in.

SYNCOFF disables the SYNC signal.

TRG [TRIGDEF] programs the voltage level threshold and logic sense or trigger condition of each channel.

TRGH [TRIGDEF] programs the voltage level threshold and logic sense or trigger condition of each channel, within the ±50V range.

TRGL [TRIGDEF] programs the voltage level threshold and logic sense or trigger condition of each channel, within the ±10V range.

VHYST [A] turns on/off the voltage compensation performed during voltage commands.

VOLT? [L],[B] returns DC voltage of the input channel.

VOLTALL? [L],[CHANNEL STRING]
takes a voltage measurement on all channels simultaneously.

VOLTALLH? [L],[CHANNEL STRING]
takes a voltage measurement within the ±50V range on all channels simultaneously.

VOLTALLL? [L],[CHANNEL STRING]
takes a voltage measurement within the ±10V range on all channels simultaneously.

VOLTAVE specifies that only the average voltage should be returned form one of the VOLT commands.

VOLTFULL specifies that the maximum, minimum, and average voltages should be returned form one of the VOLT commands.

VOLTH? [L],[B] returns the dc voltage of the specified input channel within the ±50V range.

VOLTL? [L],[B] returns the dc voltage of the specified input channel within the ±10V range.

VOLTNEXT? optional. This command is included for use with controllers which do not support successive readback.

Command Descriptions

Command: ABREV (Abbreviated readback)

Syntax: ABREV [A]

Mode: Analog

Purpose: Returns the BUF OVFLW and NO ENTRIES messages in abbreviated form when reading the event buffer.

Description: [A] must be one of the following:

[A]	Action
ON	abbreviated mode on
OFF	abbreviated mode off (default).

When reading the event buffer via the DATA? command, two special messages can be returned (a full description of these messages is given in the Event Buffer section). These are the BUF OVFLW (buffer overflow) and the NO ENTRIES messages. If abbreviated mode is enabled, these messages will be returned as a signal N and a signal B character, respectively. The VXI defined END bit will be set on each of these characters. No <CR>, nor <LF> will be appended.

Command: ANADIG (Combination Analog/Digital Mode)

Syntax: ANADIG [A]<TM>
or AD [A]<TM>

Mode: Analog or Digital

Purpose: This command selects combination Analog/Digital mode.

Description: This command sets the module so that channels 0 through 15 operate in Analog mode, and channels 16 through 31 operate in Digital mode. In this mode, the module can only be armed with the ARM ON and ARM OFF commands, not by an external signal.

[A] a single letter which defines whether Analog or Digital information is shown on the front panel display, and what type of information is returned with the DATA? command:

A analog information is displayed, and DATA? command returns analog information.

D digital information is displayed on channels 31 to 16 as if a DISPDIG BYTE 3,2 command were sent. The DATA? command returns digital information. Next time Digital mode is entered, the display will revert to the byte ordering defined by the most recent DISPDIG command.

In either case, the type of returned data can be controlled by using the DATAANA? or DATADIG? commands.

If [A] is omitted, the display shows the same information type as before this command was sent.

The state of the module changes as follows:

- Display may change as described above.
- DATA? command may now return different information as described above.
- All comparator status latches and digital input latches are cleared.
- The module becomes armed if the last ARM command specified ON. If any other option was chosen for the last ARM command, the module becomes unarmed.
- The Event buffer is cleared.
- Any channels 0 through 15 on the "wrong" side of their threshold will immediately be recorded and will generate an interrupt (if module is armed, and channel was previously enabled with EQU command).
- If this command is sent when the module is already in combination Analog/Digital mode, the only effect it will have is to change the display and readback type, if the [A] parameter is specified.

Example:	ANADIG<TM>	The module is set so that channels 0 through 15 operate in Analog mode, and channels 16 through 31 operate in Digital mode.

Command: ANALOG (Analog Mode)

Syntax: ANALOG<TM>
or A<TM>

Mode: Analog

Purpose: This command selects the Analog mode.

Description: If this command is entered from Digital mode or Combination Analog/Digital mode, the state of the module changes as follows:

- Display changes to analog information.
- DATA? command now returns analog information.
- All digital input latches and comparator status latches are cleared.
- The Armed state of this module is that given by the last ARM command (the module is unarmed on power-up).
- The Event buffer is cleared.
- Any channels on the "wrong" side of their threshold will immediately be recorded and will generate an interrupt (if the module is armed, and the channel was previously enabled with the EQU command).

This command has no effect if given when the module is already in Analog mode.

Example: ANALOG<TM> The module is now in Analog mode.

Command: APER (Aperture)

Syntax: APER [A]<TM>

Mode: Analog or Digital

Purpose: Specifies aperture time for VOLT? command.

Description: [A] the aperture time in seconds.

The default aperture time is 10 milliseconds. The relationship of the aperture time to the VOLT? command is given in Appendix E, Voltage Measurement on the VX4286.

The aperture tine may be any value between 0.02 ms and 655.35 ms.

Example: APER 0.05 sets the aperture time to 50 milliseconds.

Command: ARM (Arm)

Syntax: ARM [A]<TM>

Mode: Analog

Purpose: This command programs when to ARM the module to begin monitoring the inputs.

Description: Allowable values for [A] when in full Analog mode are:

[A]	ARM signal is taken from
0	VXI TTLTRG* 0
1	VXI TTLTRG* 1
2	VXI TTLTRG* 2
3	VXI TTLTRG* 3
4	VXI TTLTRG* 4
5	VXI TTLTRG* 5
6	VXI TTLTRG* 6
7	VXI TTLTRG* 7
±8	Front Panel
OFF or 9	Module is permanently unarmed (default)
ON or 10	Module is permanently armed

Allowable values for [A] when in Combination Analog/Digital mode are:

OFF or 9	Module is permanently unarmed (default)
ON or 10	Module is permanently armed

While the module is not armed, no data will be recorded, no interrupts will be generated due to the input signals, and the TTL output lines of analog channels will remain low (if they are not tri-stated). If [A] is ON, the module is always armed. The default condition upon power-up is unarmed.

If [A] is given with the value 0 through 8 in Combination Analog/Digital mode, the command will be ignored.

If [A] = 0 to 7, the module will not be armed until a pulse is received on the appropriate VXI trigger line (assuming the Counter Sync signal does not have control of the TTLTRG* lines via a SYNC 0-7 command). All comparator status latches are cleared upon receiving an ARM command with [A] = 0 to 7. The polarity is active low, complying with the VXIbus defined Synchronous Trigger Protocol.

If [A] = ±8, the module will not become armed until a pulse is received on the front panel connector. All comparator status latches are cleared upon receiving a ARM command with [A] = ±8. The polarity or the pulse is defined by whether [A] is positive (active high) or negative (active low).

Examples:

ARM 2<TM>	Uses TTLTRG* 2 (if SYNC 0-7 command has not been given).
ARM -8<TM>	Uses front panel Arm signal (active low).
ARM ON<TM>	Module permanently armed.
ARM OFF<TM>	Disabled External Arm signal, module is unarmed.

Command: ARM? (Arm Query)

Syntax: ARM?<TM>

Mode: Analog

Purpose: Returns whether or not the module is armed.

Description: A 1<CR><LF> is returned if the module is now armed, a 0<CR><LF> if it is not.

Example:
ARM?<TM>
1<CR><LF> The module is armed.

Command: BUF? (Event buffer Query)

Syntax: BUF?
or B?

Mode: Analog or Digital

Purpose: Returns whether the Event buffer is full or empty.

Description: A 0<CR><LF> is returned if the Event buffer is empty, a 2<CR><LF> if it is full, and a 1<CR><LF> otherwise.

The system is not required to read all three characters of response data. It may read any number from one to three characters.

Example: BUF?
1<CR><LF> The Event buffer is not full and not empty.

Command: CAL (Calibrate)

Syntax CAL [A],[B]<TM>

Mode: Analog or Digital

Purpose: Used to calibrate this module.

Description: The CAL command is used to calibrate the VX4286 Module to its published accuracy specifications. Calibration data is stored in nonvolatile memory on the VX4286. For details on the entire procedure, refer to the Calibration section in the Service Manual.

[A] is either S, A, E, or AB:

S	start
A	apply
E	end
AB	abort

The CAL S,[B] command should be sent first to signify the start of a calibration sequence, along with which channels are being calibrated. In this form of the command, [B] is a multi-character string defining which channels are to take place in the calibration. [B] has the format:

[CHANNEL],[CHANNEL],...[CHANNEL]

where [CHANNEL] is:

a channel number between 0 and 31, or

a range of channels in the form:

<number 0 to 31> TO <number 0 to 31>

There may be any number of white spaces (including zero) before and after any TO.

The CAL A,[B] command should be sent next. In this form of the command, [B] defines which voltage is being applied to the input of the channel(s) under test, as defined by the CAL S command. [B] may be -10, 10, -50, or 50. A CAL A command must be sent for each voltage. The CAL A command takes slightly under half a second for each channel specified in the CAL S command to execute.

The CAL E command specifies the end of the calibration procedure.

After the CAL E (Calibration End) command is given, this module should be read. If it returns a 64,CALIBRATION COMPLETE response, calibration was correctly performed. If it does not, there was an error during the calibration procedure. The previous calibration data will remain in effect, unchanged. Errors should be read until the 00,NO ADDITIONAL ERRORS TO REPORT message is returned, as multiple errors are possible.

The error responses are as follows:

CAL ERROR CHAN [C]: [V] VOLTAGE READS TOO LOW<CR><LF>, or
CAL ERROR CHAN [C]: [V] VOLTAGE READS TOO HIGH<CR><LF>

The device has detected that the applied voltage is at least 5% out of tolerance. [C] is the channel number, [V] is either +10, -10, +50, or −50. If multiple channels were specified with the CAL S command, then [C] represents the first channel where the out of tolerance voltage was detected.

CAL ERROR: ALL VOLTAGES NOT RECEIVED<CR><LF>

A successful CAL A command was not sent for each voltage of 10, -10, +50, and -50.

The CAL AB command may be sent at any time after a CAL S command, to terminate the calibration sequence without updating the nonvolatile RAM.

Examples:

Calibrating all channels:
CAL S,0to31<TM>
CAL A,+10<TM>
CAL A,-10.00<TM>
CAL A,+5e1<TM>
CAL A,-50<TM>
CAL E<TM>

Calibrating an individual channel (channel 2):
CAL S,2<TM>
CAL A,-10<TM>
CAL A,+10<TM>
CAL A,-50<TM>
CAL A,+50<TM>
CAL E<TM>

Calibrating a number of channels (channels 2, 4, 5, 6):
CAL S,2,4 TO 6<TM>
CAL A,-50<TM>
CAL A,+50<TM>
CAL A,-10<TM>
CAL A,+10<TM>
CAL E<TM>

Command: CAL? (Calibration Query)

Syntax: CAL?<TM>

Mode: Analog or Digital

Purpose: Returns a message specifying whether or not all channels have been calibrated.

Description: If all channels have been calibrated, the message ALL CHANNELS CALIBRATED<CR><LF> is returned. If not, it returns the message UNCALIBRATED CHANNELS: [CHANNELS], where [CHANNELS] specifies the channels. Any three or more consecutive channels will have the first and last channel separated by a dash, and all other channels will be separated by commas (see example). If all channels are not calibrated, this message will be put in the error buffer on power-up (see the ERR? command).

Example: CAL?<TM>

If channels 0, 2, 3, 4, and 7 are uncalibrated, the message returned would be:

UNCALIBRATED CHANNELS: 0,2-4,7<CR><LF>

Command: CLR (Clear Analog Latches)

Syntax: CLR<TM>
or C<TM>

Mode: Analog

Purpose: This command clears all comparator status latches.

Description: If the module is currently in Analog mode, all latches are cleared. If it is in combination Analog/Digital mode, latches corresponding to channels 0 to 15 (analog section) are cleared.

This command has no effect in Digital mode. Digital input latches may be cleared by using the command sequence ENB N; ENB;

Example: CLR<TM>

Command: DATA? (Data Query)

Syntax: DATA? [R],[Q]<TM>
or D? [R],[Q]<TM>

Mode: Analog or Digital

Purpose: In Digital mode, this command returns the values of the digital inputs or digital input latches. In Analog mode, this command returns the Event buffer, which contains all channels detected on the "wrong" side of their respective thresholds.

Description: In Digital mode, it returns the values of the digital inputs or digital input latches, in a format specified by the FMTDIG command.

In Analog mode, it returns the Event buffer, which contains all channels detected on the "wrong" side of their respective thresholds, in a format specified by the FMTANA command. Details on the Event buffer are given in the Event Buffer subsection.

This command does not have to be sent before each input request. Once this command is given, the information described above will be returned with every input request. It is necessary to send this command if time synchronization is being used, in order to update the newly synchronized time (refer to SYNC and SET commands).

[R] (for 're-enable') is optional, and has significance only in Analog mode. If R is specified, all channels that are subsequently read back will automatically be re-enabled to have information on them recorded again. If they are still on the "wrong" side of the threshold, information will be recorded again, and an interrupt will be generated. If R is omitted, the channels read back will never have their data recorded or have an interrupt generated again unless re-enabled by a EQU or REENB command (unless the Flip Continuous bit for this channel is set). If DATA? R is sent in digital mode, the R will be ignored.

[Q] (for 'eQuation period reset') is optional, and if given, clears the equation period whenever the last entry in the Event buffer is read, guaranteeing that no entries come in between the time the last entry is read and equation period is reset (refer to Appendix D for further details).

Examples:

DATA?<TM> Requesting data, channels not re-enabled.
DATA? R<TM> Requesting data, channels re-enabled.

For both examples, if the module is in Analog mode and a FMTANA IND,N,CM<CR> command had previously been sent, the data returned might be:

10,23<CR><LF>

For both examples, if the module is in Digital mode and a FMTDIG HEXA<CR> command had previously been sent, the data returned might be:

A0000109<CR><LF>

Related examples can be found under the FMTANA and FMTDIG commands.

Command: DATAANA? (Data Query - Analog Information)

Syntax: DATAANA? [R],[Q]<TM>
or DA? [R],[Q]<TM>

Mode: Analog

Purpose: Returns the Event buffer.

Description: This command operates identical to the DATA? command in Analog mode, but can be used in Combination Analog/Digital mode to force analog readback.

If this command is sent in full Digital or Analog mode, it will operate identical to the DATA? command. That is, in Digital mode, it returns the values of the digital input latches. In Analog mode, it returns the Event buffer, which contains all channels detected on the "wrong" side of their respective thresholds.

Examples: DATAANA?<TM> Requesting data, channels not re-enabled.

DATAANA? R<TM> Requesting data, channels re-enabled.

For both examples, if a FMTANA IND,N,CM,N<TM> command had previously been sent, the data returned might be:

10<CR><LF>

Related examples can be found under the FMTANA command.

Command: DATADIG? (Data Query - Digital Information)

Syntax: DATADIG? [R],[Q]<TM>
or DD? [R],[Q]<TM>

Mode: Digital

Purpose: Returns the values of the digital inputs or digital input latches.

Description: This command operates identical to the DATA? command in Digital mode, but can be used in Combination Analog/Digital mode to force digital readback.

If this command is sent in full Analog or Digital mode, it will operate identical to the DATA? command. That is, in Digital mode, it returns the values of the digital inputs or digital input latches. In Analog mode, it returns the Event buffer, which contains all channels detected on the "wrong" side of their respective thresholds.

Examples: DATADIG?<TM> Requesting data, channels not re-enabled.

DATADIG? R<TM> Requesting data, channels re-enabled.

For both examples, if a FMTDIG HEXA<TM> command had previously been sent, the data returned might be:

0109<CR><LF>

Related examples can be found under the FMTDIG command.

Command: DBENB (Debounce Enable)

Syntax: DBENB [N_1], ...[N_x]<TM>
or DE [N_1], ...[N_x]<TM>

Mode: Analog or Digital

Purpose: Enables or disables debounce of the selected inputs.

Description: This command should be used when it is desired to debounce an input. It is most useful for switch closures, where the bouncing switch would cause a channel to be recorded multiple times.

[N] specifies which groups of four inputs should have the debounce circuitry enabled. All groups not specified will have the debounce circuitry disabled (default is all groups disabled). Each group of four is dedicated to one of two debounce counter.

[N]	Channels	Debounce Counter
N	none	-- (debounce circuitry on all channels will be disabled)
0	0-3	1
1	4-7	1
2	8-11	2
3	12-15	2
4	16-19	1
5	20-23	1
6	24-27	2
7	28-31	2

If [N] is omitted, debounce circuitry on all channels will be enabled.

The debounce time is set with the DBTIME command.

Examples:

DBENB 0,3<TM>	enables debounce circuitry for channels 0-3 and 12-15; disables circuitry for channels 4-11 and 16-31.
DBENB N<TM>	disables debounce circuitry for all channels. This is the default condition.
DBENB 2<TM>	enables debounce circuitry for channels 8-11; disables circuitry for channels 0-7 and 12-31.
DBENB<TM>	enables debounce circuitry for all channels.

Command: DBTIME (Debounce Time)

Syntax: DBTIME [A],[B]<TM>
or DT [A],[B]<TM>

Mode: Analog or Digital

Purpose: Specify debounce time for channels using debounce circuitry.

Description:

[A] specifies whether debounce counter 1 or 2 is to have its time changed. Debounce counter 1 operates on channels 0 to 7, and 16 to 23. Debounce counter 2 operates on channels 8 to 15 and 24 to 31. They are divided into four sections so that both counters will be available to the Analog section in Combination Analog/Digital mode (ANADIG command).

[B] specifies the time, in seconds, that the input voltage may toggle about the threshold, and still only record this channel a single time (and generate a single interrupt). Any signal that does not stay on the "wrong" side of the threshold for time [B] will not be recorded. Any signal that stays on the "wrong" side for the time 2*[B] or longer will be recorded. Any signal staying on the "wrong" side between time [B] and 2*[B], may or may not be recorded. [B] may be any time between .0001 to 6.5535 seconds.

The enabled channels are specified by the DBENB command.

Example:

DBTIME 1,.01<TM>	Sets the debounce time to 10 msecs for all channels 0 to 7 or 16 to 23 that have their debounce circuitry enabled (DBENB command).
DBTIME 2,.3<TM>	Sets the debounce time to 300 msecs for all channels 8 to 15, and 24 to 31, that have their debounce circuitry enabled (DBENB command).

Command: DIGITAL (Digital Mode)

Syntax: DIGITAL<TM>
or D<TM>

Mode: Digital Mode

Purpose: This command selects the Digital mode.

Description: The state of the module changes as follows:

- display changes to digital information, with byte ordering as defined by the most recent DISPBYTE command,
- DATA? command now returns digital information,
- all digital input latches and comparator status latches are cleared, and
- the strobe state is defined by last STB command received (STB S excluded).

This command has no effect if the module is already in Digital mode.

Example: DIGITAL<TM>

Command: DINT (Disable Interrupts)

Syntax: DINT [A]<TM>

Mode: Analog or Digital

Purpose: This command disables generation of the VXIbus Request True interrupts.

Description: The DINT command disables generation of VXIbus Request True interrupts. Interrupts occur either when the equation sent with the EQU command becoming true (EQU), or when an error occurs (ERR).

[A] can take one of two forms. If [A] is sent as a number, it is as follows:

[A]	Specifies
1	EQU interrupt disabled
2	ERR interrupt disabled
3	both EQU and ERR interrupts disabled

[A] may also be sent as the string EQU and/or ERR, defining which interrupt to disable. To disable both interrupts, use a comma to separate the two terms (see the third example below).

For further information of interrupts due to their voltage states, refer to the EQU command. For further information on programming errors, refer to the ERR? command.

Example:

DINT EQU<TM>	EQU interrupts are disabled.
DINT ERR<TM>	ERR interrupts are disabled.
DINT EQU,ERR<TM>	Both EQU and ERR interrupts are disabled.
DINT 1<TM>	EQU interrupts are disabled.
DINT 3<TM>	Both EQU and ERR interrupts are disabled.

Command: DISPANA (Display in Analog Mode)

Syntax: DISPANA [A],[B]<TM>
or DART<TM> DISPLAY ANALOG REALTIME
or DALP<TM> DISPLAY ANALOG LATCH PRIORITY
or DALL<TM> DISPLAY ANALOG LATCH LATEST

Mode: Analog

Purpose: Defines how the data is to be presented on the front panel display during Analog mode.

Description: [A] a string which specifies where the data is sampled. [A] must be one of the following:

REALTIME the displayed data is based upon the level of the signals at their inputs sampled every ¼ of a second. In this instance, the [B] parameter should not be specified.

LATCH the displayed data is based upon the comparator status latches. The latches contain all channels that have transitioned since the last re-enable time. In this case, the [B] parameter should be specified.

[B] a string specifying which data is sampled. [B] must be one of the following:

PRIORITY the highest priority of the comparator status latches (see DISPPRI command) will be displayed. Once a channel is put on the display in this mode, it will remain until either a channel with higher priority goes to the "wrong" side of its threshold, or a RST DISP or another DISPANA command is sent.

LATEST the last one that was set will be displayed. It is important to note with the LATEST option that if two channels change state within a period of time tag uncertainty (see Specification section), either channel may be displayed, even though the displayed channel may have come slightly (within a period of time tag uncertainty) ahead of the other.

The name of a channel is displayed when its input voltage is on the "wrong" side of its threshold. Only channels enabled with the DISPENB command are displayed. If no channels are displayed, the display will be set to all dashes.

The DART command is an abridged version of DISPANA REALTIME, DALP stands for DISPANA LATCH PRIORITY, and DALL stands for DISPANA LATCH LATEST.

Examples: DISPANA REALTIME<TM>
or DART<TM> This will display the highest priority of any channel inputs that are on the "wrong" side of their programmed voltage threshold, sampled every ¼ second.

DISPANA LATCH,PRIORITY<TM>
or DALP<TM> The display will have the highest priority of any channels that have transitioned between the time this command is received until another DISPANA or RST DISP command is sent, or a channel of a higher priority goes to the "wrong" side of its threshold.

DISPANA LATCH,LATEST
or DALL<TM> The display will have the latest channel to have gone to the "wrong" side of its threshold.

Command: DISPBYTE (Display Byte)

Syntax: DISPBYTE [N],[M]<TM>
or DB [N],[M]<TM>

Mode: Digital

Purpose: Defines which bytes of data are to be displayed on the front panel display during Digital Mode.

Description: [N] defines the byte displayed on the leftmost two digits of the display in hexadecimal.

[M] defines the byte displayed on the rightmost two digits of the display in hexadecimal.

[N] or [M]	Display Bits:
3	31-24
2	23-16
1	15-8
0	7-0

Example: DISPBYTE 1,3<TM> would display channels 15 through 8 on the left two digits of the display, and channels 31 through 24 on the rightmost digits.

Command: DISPDIG (Display in Digital Mode)

Syntax:
DISPDIG [A]<TM>
or DDRT<TM> DISPLAY DIGITAL REALTIME
or DDL<TM> DISPLAY DIGITAL LATCHED

Mode: Digital

Purpose: Defines how the data is to be presented on the front panel display during Digital Mode.

Description: [A] a string which specifies where the data is sampled. [A] must be one of the following:

REALTIME the displayed data is based upon the level of the signals at their inputs sampled every 1/4 of a second.

LATCH the current value of the digital input latches are displayed. The digital input latches are the value of the inputs on the last strobe (or last read of data if STB RD option was chosen).

The DDRT command is a short version of DISPDIG REALTIME, and DDL stands for DISPDIG LATCH.

Examples:
DISPDIG REALTIME<TM>
or DDRT<TM> This will display 16 bits of input data.

DISPDIG LATCH<TM>
or DDL<TM> This will display 16 bits of digital input latches. The digital input latches contain data latched in during the last strobe (or last read of data if the STB RD option was chosen).

Command: DISPENB (Display Enable)

Syntax: DISPENB [A]<TM>
or DI [A]<TM>

Mode: Analog

Purpose: Defines the set of channels that may be displayed in Analog mode.

Description: Any channel not given in this command will not be displayed in Analog mode.

[A] can take one of two forms.

If [A] is the string EQU, the enabled channels for the display will directly follow the channels given by the EQU command.

Otherwise, [A] is a multi-character string defining which channels are enabled for displaying. [A] has the format:

[CHANNEL],[CHANNEL],...[CHANNEL]

where [CHANNEL] is:
a channel number between 0 and 31, or
a range of channels in the form:
<number 0 to 31> TO <number 0 to 31>

There may be any number of white spaces (including zero) before and after any TO.

The default condition upon power-up is DISPENB EQU.

Example: DISPENB 3,4,6 TO 30<TM>
If any channel 3, 4, and 6 through 30 meet the criteria for being displayed, the channel will be displayed. If the criteria is not met, the display will contain four underscore (_) characters, even if another channel meets the criteria. For example, if the display mode is "display last latched channel", and channel 5 is the last latched channel, the display will contain four underscore characters.

DISPENB EQU<TM> Any enabled channel (any channel given within the last EQU command) will be displayed if that channel meets the criteria for being displayed.

Command: DISPPRI (Display Priority)

Syntax: DISPPRI [CHANNEL STRING]<TM>
or DP [CHANNEL STRING]<TM>

Mode: Analog

Purpose: Defines the priority of the channels for the display in Analog mode.

Description: [CHANNEL STRING] is a multicharacter string defining the priority of the channels. [CHANNEL STRING] has the format:

[CHANNEL],[CHANNEL],...[CHANNEL]

where [CHANNEL] is:

a channel number between 0 and 31, or
a range of channels in the form:
<number 0 to 31> TO <number 0 to 31>

There may be any number of white spaces (including zero) before and after any TO.

If [CHANNEL STRING] is omitted, the priority will be as if a DISPRI 0 TO 31 command had been sent (channel 0 highest).

The name of a channel is displayed when its input voltage is on the "wrong" side of its threshold.

The default condition on power-up is DISPPRI 0 TO 31 (channel 0 highest).

Example:

DISPPRI 3,4,31 TO 5,2TO0<TM> The priority will be as follows (highest priority first):

3, 4, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 2, 1, 0

DISPPRI 3,4,31 TO 0<TM> The priority will be the same as the previous example. Note that a channel may be specified twice (channel 3 is specified initially, and again in 31 TO 0), with the first occurrence having precedence.

DISPPRI 31 TO 0<TM> The priority will be as follows (highest priority first):

31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

DISPPRI 0 TO 31<TM> The priority will be as follows (highest priority first):

0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31

DISPPRI 5,17<TM> The priority will be as follows (highest priority first):

5, 17, 0, 1, 2, 3, 4, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 18, 19, 20,
21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31

Command: ENB (Digital Channel enable)

Syntax: ENB [CHANNEL STRING]<TM>

Mode: Digital

Purpose: This command is used to enable any bit and corresponding TTL output in Digital mode.

Description: [CHANNEL STRING] is a multicharacter string defining which channels are to be enabled. [CHANNEL STRING] has the format:

[CHANNEL],[CHANNEL],...[CHANNEL]

where [CHANNEL] is:

a channel number between 0 and 31, or
a range of channels in the form:
<number 0 to 31> TO <number 0 to 31>

[CHANNEL STRING] may optionally be a single character 'N', which specifies that no channels are enabled.

There may be any number of white spaces (including zero) before and after any TO.

If [CHANNEL STRING] is omitted, all channels will be enabled as if an ENB 0 TO 31 command had been sent.

The default on power-up is all bits enabled. Any bit that is disabled will be in the zero state when displayed or when the digital input latches are read back with the DATA? command. The TTL output for this channel will be permanently low (if the output is not tri-stated with the OUTPUT command).

Example: ENB 5,7,11<TM> enables channels 5, 7, and 11.

ENB 4,8 to 12<TM> enables channel 4 and channels 8 through 12.

Command: EQU (Equation/Analog Channel enable)

Syntax: EQU [F],[E],[EQUATION]<TM>
or E [F],[E],[EQUATION]<TM>

Mode: Analog

Purpose: The EQU command defines the condition (with a Boolean equation) that will cause a Request True interrupt to be generated and the EQU OUT signal to pulse. It also specifies which channels are enabled or disabled for collection in the Event buffer during Analog Mode.

Description: [EQUATION] is a multicharacter string defining the condition under which a Request True interrupt occurs and the EQU OUT signal pulses, and which channels are to be enabled. [EQUATION] has the format:
[CHANNEL][OPERATOR][CHANNEL][OPERATOR] ...

where [CHANNEL] is:
a channel number between 0 and 31, or
a range of channels in the form:
<number 0 to 31> TO <number 0 to 31>

[OPERATOR] is either + or * :
+ the OR operator
* the AND operator.

[EQUATION] can optionally be a single character 'N', which specifies that all channels are disabled.

If [EQUATION] is omitted, all channels are enabled as if a EQU 0 TO 31 command had been sent.

There may be any number of white spaces between operators of channels. The * operator has a higher priority then the + operator. In other words, EQU 3 * 4 + 2 * 5<TM> will interrupt in the case where both 3 and 4 OR the case where 2 and 5 are detected on the "wrong" side of their respective thresholds. The maximum number of terms that include a * is 32. For compatibility with other commands, a comma (,) may be used in place of any + .

Any channel not included in [EQUATION] is disabled. Any channel included is enabled.

For details on the Event buffer, see the Event Buffer section.

[F] (for 'force') is optional and defines whether to force enabling of all specified channels. If [F] is omitted, only the specified channels that are not already residing in the Event buffer will be enabled. This is the normal use, and guarantees that multiple entries of the same channel do not exist in the Event buffer at the same time (unless of course the Flip Continuous bit on a channel is set). If [F] is specified, all specified channels are enabled independent of whether or not they exist in the Event buffer. (This does not guarantee only one entry of a channel exists in the buffer at a time, since a transition can occur between the

time the last entry is read from the Event buffer and the time this command is sent.)

[E] (for 'Event buffer clear') is optional. If given, it clears the Event buffer before executing the EQU command as if a RST EVNT;EQU command sequence were given. The difference is that the [E] option guarantees that no channels are recorded between the Event buffer clearing and the enabling process (refer to Appendix D for further details).

The Request True interrupt and EQU OUT signal become active whenever an enabled channel is detected on the "wrong" side of its threshold IF the equation has been satisfied at this point. Note that the equation defines events over a period of time, and not the case where all events occur simultaneously at the same time (where an event is the detection of a channel on the "wrong" side of its threshold). The period of time becomes active (all events cleared) with the reception of any EQU command. Details on how to reset the equation are given in Appendix D.

The default condition on power-up is that all channels are disabled.

Example:

EQU 0+31 *23 + 4 + 5 + 10 TO 22 + 25*26 * 27<TM>

Would interrupt if channels 0 or 4 or 5, or any channel from 10 to 22, or both channel 23 and 31, or channels 25 and 26 and 27 have been detected on the "wrong" side of their respective thresholds, at any time after this command is received (refer to Appendix D). Channels 1, 2, 3, 6, 7, 8, 9, 24, 28, 29, and 30 are all disabled from causing an interrupt and from being recorded, as they are not included in the equation.

EQU N<TM> All channels are disabled from causing an interrupt and being recorded.

EQU 0 TO 31<TM>

Any channel being on the "wrong" side of its respective threshold will be recorded and cause an interrupt.

EQU F,0 TO 20 + 22 TO 31<TM>

Any channel being on the "wrong" side of its respective threshold except channel 21 will be recorded and cause an interrupt. Channels except 21 are enabled at this time, independent of whether they presently exist in the Event buffer.

EQU 23 + 23*24<TM>
EQU 23*24 + 23<TM>

Unsimplified equations will be accepted. Both of these equations reduce to EQU 23<TM>, which will cause recorded data and cause an interrupt ONLY if channel 23 is detected on the "wrong" side of its threshold.

EQU E,1*23 + 02*23<TM>

If channels 1, 2, or 23 are on the "wrong" side of their respective thresholds, they will be recorded. An interrupt will occur if channels 1 and 23 or if channels 2 and 23 are detected on the "wrong" side of their respective thresholds. The Event buffer will first be cleared.

Command: EQURST (Equation Reset)

Syntax: EQURST<TM>
or ER<TM>

Mode: Analog

Purpose: Resets the equation period.

Description: This command resets the equation period. For further details, refer to Appendix D.

Command: EQUPOL (EQU OUT Polarity)

Syntax: EQUPOL [A]<TM>
or EP [A]<TM>

Mode: Analog

Purpose: The EQUPOL command sets the polarity of the EQU OUT signal.

Description: [A] must be either + or - :

+ the EQU command will be a positive pulse.
- the EQU command will be a negative pulse.

The negative pulse is recommended for systems which may be reset during a test, as this line will revert to a HIGH level upon a reset.

Example: EQUPOL -<TM> EQU OUT signal will be active low.

Command: ERR? (Error Query)

Syntax: ERR?<TM>
or E?<TM>

Mode: Analog or Digital

Purpose: The ERR? command instructs this module to return its error status next time input is requested from the module.

Description: Errors reported by this command include those detected during self test.

All errors listed in this section cause a Request True interrupt to be generated (if interrupts are enabled by the INT command), and the ERR LED to be lit.

All errors occurring since the last ERR? command or reset condition will be returned, beginning with the first error found. After issuing the ERR? command to the VX4286, the system controller should continue to request input from the module until the 00,NO ADDITIONAL ERRORS TO REPORT message is returned from the module. The ERR LED will go out when the last error is read. The ERR? command may be sent before each input request.

This command does not have to be sent before each input request. Once this command is given, the Error buffer will be returned with each input request.

Response Syntax:

The format of data returned by the ERR? command is:

[error],[english message]<CR><LF>

where:

[error] is a 2-digit error code.

[english message] is an English message describing the error.

Examples: The two-digit error codes, their message, and meaning are as follows:

00,NO ADDITIONAL ERRORS TO REPORT
There are no more errors to report.

10,UNCALIBRATED CHANNELS: [CHANNELS]
This specifies which channels are uncalibrated during self test. [CHANNELS] specifies the uncalibrated channels. Any three or more consecutive channels will have the first and last channel separated by a dash, and all other channels will be separated by commas. An example would be UNCALIBRATED CHANNELS: 0,2-4,6,7,23.

11,INOPERATIONAL NOVRAM
During a reset or power-up self test, the nonvolatile RAM holding the calibration factors was found not to be working correctly. In this case, the

UNCALIBRATED CHANNELS: 0-31 error will also be reported. All channels will still operate correctly, but their accuracy could be off as much as 5%.

12,NOVRAM BLOCK CHECK ERROR

During a reset or power-up self test, the data in the nonvolatile RAM holding the calibration factors was found to be corrupt. Upon finding this situation, the nonvolatile RAM is reprogrammed with default calibration data. The 10,UNCALIBRATED CHANNELS: 0-31 error will also be reported. All channels will still operate correctly, but their accuracy could be off as much as 5%.

13,INOPERATIONAL SLAVE MICROPROCESSOR

This module has two processors onboard, a master and a slave microprocessor. This error is generated during self test when the slave microprocessor is nonfunctional. If this occurs, the VXI interface will still function, but all channels will be nonfunctional.

14,FPGA WILL NOT PROGRAM CORRECTLY

During a reset or power-up self test, the onboard FPGAs (Field Programmable Gate Arrays) were found not to be operating properly.

15,CHANNELS FAILED [VOLT]V TEST: [CHANNEL]

During self test, one or more channels was found to be more then 5% out of specification when tested with an onboard voltage source at [VOLT] volts. [VOLT] can be either +12V, +6V, 0V, -6V, or -12V. [CHANNELS] specifies the channel(s) in error, and has the same syntax as the 10,UNCALIBRATED CHANNELS: error described above.

20,VOLTAGE OVERRANGE

The voltage specified in the TRG or TRGH commands is not between -50 and +50 volts, or the voltage specified in the TRGL command is not between -10 and +10 volts.

21,SPECIFIED [COMMAND] TIME EXCEEDS MAXIMUM OF [SECS] SECS

[COMMAND] is either DEBOUNCE or APERTURE. This indicates that the time sent exceeded 6.5535 seconds for the DEBOUNCE command, or 0.65535 seconds for the APER command.

22,VOLT? COMMAND MAY NOT WORK WITH DEBOUNCE ENABLED

A VOLT? command was given on a channel that has its debounce circuitry enabled. The debounce circuitry in this case acts like a filter, which may cause unexpected results to be returned.

30,INVALID [COMMAND] OPTION [VALUE]

A number [VALUE] sent with the [COMMAND] command is invalid for this command.

31,INVALID PARAMETER TO THE [COMMAND] COMMAND

A parameter sent with the [COMMAND] command is invalid for this command.

32,INVALID DEBOUNCE COUNTER SPECIFIED

A debounce counter other than 1 or 2 has been specified.

33,INVALID YEAR SPECIFICATION
The year given with the SET DATE command is in improper form.

34,ILLEGAL CHAN [CHAN]
A channel [CHAN] greater than 31 has been specified.

40,UNRECOGNIZED COMMAND
The received command is unrecognized.

41,RECEIVED UNEXPECTED [CHAR] WHILE [REASON]
[CHAR] = [single quote][character][single quote] for printable characters (20 hex through 7f hex), for example 'G'.
or
[CHAR] = [SP][ASCII hex digit][ASCII hex digit] for non-printable characters (00 hex through 19 hex and 80 hex through FF hex), for example, 0A.

[REASON] = one of the following:
- EXPECTING A LINE FEED, SEMICOLON OR COMMA.
- EXPECTING A NUMERIC.
- PARSING MANTISSA.
- PARSING EXPONENT.

42,TOO MANY DIGITS IN EXPONENT
More than three digits were received in an exponent.

43,ADDITIONAL CHARACTER AFTER CLOSING QUOTE OF NAME COMMAND
When giving the name in the NAME command, an extra character was found after the closing quote of the name string.

44,THE WORD TO NOT ALLOWED IN THIS POSITION OF EQU COMMAND
A TO was found in the incorrect place within the EQU command.

50,MAXIMUM NUMBER OF TERMS (32) HAS BEEN EXCEEDED
The maximum number of terms with a * in it within the EQU command is 32. If this value is exceeded, this error is generated.

51,TOO MANY CHANNELS SPECIFIED IN DISPPRI COMMAND
More than 32 channels were specified in the DISPPRI command.

52,TOO MANY VOLTAGES SPECIFIED IN TRIGGER COMMAND
More than two voltages were received in the TRG, TRGL or TRGH command.

60,MUST BE IN CALIBRATION MODE TO EXECUTE THIS COMMAND
A CAL A, CAL E, or CAL AB was received before a CAL S command.

61,INVALID VOLTAGE TO CAL COMMAND
A voltage other than +10, -10, +50, or -50 was received with the CAL A command.

Command: FLIPCONT (Flip Continuous)

Syntax: FLIPCONT [CHANNEL STRING]<TM>
or FC [CHANNEL STRING]<TM>

Mode: Analog

Purpose: This command continually reverses the trigger sense (polarity) of a particular channel, each time a channel is detected on the 'wrong' side of its threshold.

Description: [CHANNEL STRING] is a multicharacter string defining which channels are to have their trigger sense continually flipped. [CHANNEL STRING] has the format:
[CHANNEL],[CHANNEL],...[CHANNEL]

where [CHANNEL] is:
a channel number between 0 and 31, or
a range of channels in the form:
<number 0 to 31> TO <number 0 to 31>

There may be any number of white spaces (including zero) before and after any TO.

Any channels which already have their Flip Continuous bit set will be unaffected.

If [CHANNEL STRING] is omitted, all channels are set to flip continuously as if a FLIPCONT 0 TO 31 had been sent.

This command may completely fill up the Event buffer if the input signal is continually transitioning about the programmed threshold. This can create a condition where no more transitions will be recorded until the data is read back. Should this occur, the Event buffer will be re-enabled with each entry read back via the DATA? or DATA? R command. The time tag of the entries collected when the Event buffer is re-enabled will represent the re-enable time, and not the time the transition occurred. For further details, refer to the Event Buffer sub-section.

Examples: FLIPCONT 2TO4,30<TM> trigger sense changes immediately upon each transition of channel 2, 3, 4 or 30.

Command: FLIPDIS (Flip Disable)

Syntax: FLIPDIS [CHANNEL STRING]<TM>
or FDS [CHANNEL STRING]<TM>

Mode: Analog

Purpose: This command disables the flip capability of a specified channel.

Description: [CHANNEL STRING] is a multicharacter string defining which channels are to have their flip capability disabled. [CHANNEL STRING] has the format:
[CHANNEL],[CHANNEL],...[CHANNEL]

where [CHANNEL] is:
a channel number between 0 and 31, or
a range of channels in the form:
<number 0 to 31> TO <number 0 to 31>

There may be any number of white spaces (including zero) before and after any TO.

Any channels which already have their Flip bits reset will be unaffected.

If [CHANNEL STRING] is omitted, the Flip bits on all channels are reset as if a FLIPDIS 0 TO 31 had been sent.

The continuous flip (FLIPCONT command) capability will be disabled.

Examples:

FLIPDIS 30, 2 TO 4<TM>	flip capability is disabled on channels 2, 3, 4, and 30.

Command: FMTANA (Format of Analog data)

Syntax: FMTANA [A],[B],[C],[D],[E]<TM>
or FA [A],[B],[C],[D],[E]<TM>

Mode: Analog

Purpose: This command defines the format of the Event buffer, which is returned by the DATA? command when in Analog mode.

Description:
[A] specifies format of channel data
[B] specifies whether to include polarity information, level information, or an optional descriptor character [OC].
[C] specifies whether collected channel data should be returned by individual events, or cumulatively.
[D] specifies type of time tagging (relative, absolute, or none)
[E] specifies time tag format

The data format of a normal data message in Analog mode is as follows:

[OC][TIME TAG]:<SP>[CHANNEL DATA]<CR><LF>

Returning time tag is optional. Further details on this format can be found in the Event Buffer sub-section.

Parameters [B] through [E] are optional. If not given, the omitted portion of the format will remain at its last programmed value. If [C] is given, [B] must be given; if [D] is given, [B] and [C] must be given; and if [E] is given, [D],[C] and [B] must be given.

[A]	Channel data returned:
HEXA	in 8-digit ASCII hexadecimal (4-digit ASCII hexadecimal in Combination Analog/Digital mode)
HEXS	in 8-digit ASCII hexadecimal with spaces between every two digits (4-digit ASCII hexadecimal in Combination Analog/Digital mode)
BIN	in 32-bit binary (16-bit in Combination Analog/Digital mode)
BINN	in 32-bit binary (16-bit in Combination Analog/Digital mode). <CR><LF> is not returned in this case. The END bit will be asserted with the last byte of binary data.
BINC	in 32-bit binary (16-bit in Combination Analog/Digital mode). A space character is included before the binary data.
BINNC	in 32-bit binary (16-bit in Combination Analog/Digital mode). A space character is included before the binary data, and <CR><LF> is not returned in this case. The END bit will be asserted with the last byte of binary data.
BINA	in 32-bit ASCII binary (16-bit in Combination Analog/Digital mode)
BINS	in 32-bit ASCII binary with spaces between every eight digits (16-bit in Combination Analog/Digital mode)
IND	by individual channel numbers.
NAME	by individual channel names.

The BINC and BINNC options are provided so that binary data without time tag can be differentiated from Buffer Overflow and No Entries message (refer to Event Buffer sub-section).

[B] defines

- whether or not to return polarity information (whether it was above or below threshold);
- whether or not to return level information (whether a channel was captured because it was enabled or because it transitioned);
- whether or not to include an optional character at the beginning of each line. This character is listed as [OC] in the data format specification at the beginning of this command description.

Polarity is indicated in the IND and NAME formats by the inclusion of a + or - character before each channel (+ indicates the signal is above the threshold, - below). It is indicated in all other formats by the inclusion of a 32 bit mask (16 bit in combination analog/digital mode) following the channel information (a 1 indicates above the threshold). The mask is in the same format as specified by [A].

Level information is indicated in the IND and NAME formats by a character immediately after each number. If this is a space character, this channel has just transitioned to the "wrong" side of the threshold. In this case, the time tag is the transition time. If this is an 'L' character, this channel was found on the "wrong" side of the threshold upon being enabled or re-enabled. In this case, the time tag is the enable time. A channel is enabled/re-enabled under the following conditions:

- EQU command (if specified channels are going from disabled state to enabled state)
- DATA? R or REENB command (specified channels only)
- TRG command (specified channels only)
- on this module becoming ARMED
- transitioning into Analog or combination Analog/Digital mode, if the module is armed (ANALOG or ANADIG command)
- on reading an entry from a full Event buffer
- on an RST command with EQU or VOLT specified, or an RSTX command without EQU or VOLT specified

Level information is indicated in all other formats by the inclusion of a 32 bit mask (16 bit in Combination Analog/Digital mode) following the channel information (or polarity information, if specified) (a 1 indicates the same meaning as the 'L' character mentioned above). The mask is in the same format as specified by [A].

An optional character [OC] may be added to the beginning of each entry to give additional information about the entry. The character 'L' indicates that this is the last entry in the event buffer. The 'L' character is returned only with EV option (returning data by individual events) of this command. The character 'V' indicates that a buffer overflow condition occurred. The 'V' character is returned only with the CM or CMV option of this command (returning cumulative data). A space character is returned in all other cases. When the optional character is used, the type of message can be determined by the first character of the message:

[OC]	Description
L	last entry in event buffer
V	buffer overflow (cumulative report)
B	buffer overflow (individual report)
N	no entries

<SP> normal entry (additional entries exist in event buffer)

'B' and 'N' are the first characters of the BUFFER OVERFLOW, and NO ENTRIES messages described in the event buffer section.

Parameter [B] is a combination of any of the following characters.

P	return polarity information
L	return level information
O	return [OC] character
N	return none of above (N character used by itself)
S	include a space between channel, polarity, and level information in all channel data formats ([A] parameter) except IND and NAME.

For example, for polarity and level information, the string PL or LP would be used. For no polarity information, no level information, and no [OC] character, a single N would be used.

[C] defines whether the data is returned as separate events as they occurred or as a cumulative report of all occurrences since the last time the data was read.

[C]	Data returned as:
EV	individual events
CM	cumulative report
CMV	cumulative report, include an extra character at the beginning of each line to indicate if a buffer overflow condition occurred. This character, (listed as [OC] in the format specification at the beginning of this command description), is a 'V' if a buffer overflow condition occurred, and a space (20 hex) otherwise. Note that using the O option for parameter B has the same effect as using this CMV option.

[D] defines whether or not to include time tag information. If option [D] = N, time tag information will not be included in the returned messages. If [D] = REL or ABS, time tag information may be specified in either relative or absolute time, respectively. The absolute time represents the current time (specified with SET command). If the SET command has not been given, the time is relative to reset or power-up. Relative time is the time since the time tag of the last message reported. If [C] = EV, a time tag is given for each event. If [C] = CM, a time tag is given for the first event that occurred in this report.

[D]	Data returned with:
N	no time tag
REL	time tag - relative time (not fixed field)
RELF	time tag - relative time (fixed field)
ABS	time tag - absolute time (not fixed field)
ABSF	time tag - absolute time (fixed field)

[E] specifies the time tag format.

[E]	Time tag returned in:
TMSEC	integer number of 1/10s of milliseconds.
MSEC	floating point number of seconds as follows: <msecs>.<1 digit 1/10s of msecs>
SEC	floating point number of seconds as follows: <secs>.<4 digit 1/10s of seconds>
DHMS	days, hours, minutes, seconds as follows: <2 digit days>:<2 digit hours>: <2 digit minutes>:<2 digit seconds><dec pt> <4 digit 1/10s of msecs>
DATE	date as follows: <2 digit month>/<2 digit day>/<2 digit year> <2 digit hours>:<2 digit minutes>:<2 digit seconds><dec pt><4 digit 1/10s of msecs>
BIN8	binary, eight bytes. The least significant bit is equivalent to 1/10 millisecond. The colon followed by a space, which typically precedes the time tag in normal messages, is omitted in this case. If a SET DATE command had previously been sent, this time is relative to 12:00AM Jan 1, 1980.
BIN4	Identical to BIN8, except that four bytes of time tag are returned rather than eight. Four bytes can represent a time of up to 4.97 days.

The default setting is FMTANA IND,PL,EV,REL,SEC.

Example: Following are examples of what the response data to the DATA? or DATA? R command would be according to the given FMTANA command.

Assume at the time the channels were enabled (with a EQU command, 9.000 seconds after reset), channel 8 was already on the "wrong" side of its threshold. Assume also a transition to the "wrong" side of threshold on channels 31 and 29 occurred 17.109 seconds after reset, a transition on channel 0 occurred 17.123 seconds after reset, and on channel 3 at 17.233 seconds after reset. Channel 29 is programmed to record data for a voltage that is greater than the threshold, while channels 0, 3, 8, and 31 are programmed for a voltage less then their respective thresholds.

Example of Default Format

FMTANA IND,PL,EV,REL,SEC<TM> individual with polarity and level information / by event / relative seconds

9.0000: -08L<CR><LF>
7.1090: +29 ,-31 <CR><LF>
0.0140: -00 <CR><LF>
0.1100: -03 <CR><LF>
NO ENTRIES<CR><LF>

Examples of Different Channel Formats

FMTANA BIN,N,CM,N<TM> binary (the four character binary representation is represented here by four hex values within brackets < >)

<A0><00><01><09><CR><LF>

FMTANA BINN,N,CM,N<TM> binary, no carriage return, line feed (the four character binary representation is represented here by four hex values within brackets < >)

<A0><00><01><09>

FMTANA BINC,N,CM,N<TM> binary, add initial character (the four character binary representation is represented here by four hex values within brackets < >)

<SP><A0><00><01><09><CR><LF>

FMTANA BINNC,N,CM,N<TM> binary, no carriage return, line feed, add initial character (the four character binary representation is represented here by four hex values within brackets < >)

<SP><A0><00><01><09>

FMTANA BINA,N,CM,N<TM> ASCII binary

10100000000000000000000100001001<CR><LF>

FMTANA BINS,N,CM,N<TM> ASCII binary with spaces

10100000 00000000 00000001 00001001<CR><LF>

FMTANA HEXA,N,CM,N<TM> ASCII hex

A0000109<CR><LF>

FMTANA HEXS,N,CM,N<TM> ASCII hex with spaces

A0 00 01 09<CR><LF>

FMTANA HEXA,PL,CM,N<TM> ASCII hex with polarity and level information
A000010920000000000000100<CR><LF>

FMTANA HEXA,PLS,CM,N<TM> ASCII hex with polarity and level information
A0000109 20000000 00000100<CR><LF>

FMTANA HEXS,P,CM,N<TM> ASCII hex with polarity information
A0 00 01 09 20 00 00 00<CR><LF>

FMTANA HEXS,L,CM,N<TM> ASCII hex with polarity information
A0 00 01 09 00 00 01 00<CR><LF>

FMTANA IND,N,CM,N<TM> individual
00,03,08,29,31<CR><LF>

FMTANA NAME,PL,CM,N<TM>
name with polarity and level information
-CH00, -CH03, -CH08, +CH29, +CH31<CR><LF>

Examples returned by individual events

FMTANA IND,N,EV,N<TM> individual / by event
08<CR><LF>
29,31<CR><LF>
00<CR><LF>
03<CR><LF>
NO ENTRIES<CR><LF>

FMTANA IND,P,EV,N<TM> individual with polarity information / by event
-08<CR><LF>
+29,-31<CR><LF>
-00<CR><LF>
-03<CR><LF>
NO ENTRIES<CR><LF>

FMTANA IND,PL,EV,N<TM> individual with polarity and level information / by event

-08L<CR><LF>
+29,-31 <CR><LF>
-00 <CR><LF>
-03 <CR><LF>
NO ENTRIES<CR><LF>

Examples of Different Time Tags

FMTANA IND,N,EV,ABS,TMSEC<TM> individual / by event / absolute tenths of milliseconds

90000: -08<CR><LF>
171090: +29,-31<CR><LF>
171230: -00<CR><LF>
172330: -03<CR><LF>
NO ENTRIES<CR><LF>

FMTANA IND,N,EV,ABSF,TMSEC<TM> — individual / by event / absolute tenths of milliseconds, fixed field

```
 90000: -08<CR><LF>
171090: +29,-31<CR><LF>
171230: -00<CR><LF>
172330: -03<CR><LF>
NO ENTRIES<CR><LF>
```

FMTANA IND,N,EV,ABS,MSEC<TM> — individual / by event / absolute time tag in tenths of milliseconds

```
 9000.0: 08<CR><LF>
17109.0: 29,31<CR><LF>
17123.0: 00<CR><LF>
17233.0: 03<CR><LF>
NO ENTRIES<CR><LF>
```

FMTANA IND,N,CM,ABS,SEC<TM> — individual / cumulative / absolute time tag in seconds

```
9,0000: 00,03,08,29,31<CR><LF>
```

FMTANA IND,N,EV,ABS,DHMS<TM> — individual/ by event / absolute time tag in days:hours:mins:secs

```
00:00:00:09.0000: 08<CR><LF>
00:00:00:17.1090: 29,31<CR><LF>
00:00:00:17.1230: 00<CR><LF>
00:00:00:17.2330: 03<CR><LF>
NO ENTRIES<CR><LF>
```

FMTANA IND,N,EV,REL,DHMS<TM> individual / by event / relative time tag in days:hours:mins:secs

00:00:00:09.0000: 08<CR><LF>
00:00:00:08.1090: 29,31<CR><LF>
00:00:00:00.0140: 00<CR><LF>
00:00:00:00.1100: 03<CR><LF>
NO ENTRIES<CR><LF>

FMTANA BIN,N,EV,REL,DHMS<TM> binary / by events / relative time tag in days:hours:mins:secs (The four character binary representation is represented here by four hex values within brackets < >)

00:00:00:09.0000: <00><00><01><00><CR><LF>
00:00:00:08.1090: <0A><00><00><00><CR><LF>
00:00:00:00.0140: <00><00><00><01><CR><LF>
00:00:00:00.1100: <00><00><00><08><CR><LF>
NO ENTRIES<CR><LF>

FMTANA IND,N,CM,ABS,DHMS<TM> individual / cumulative / absolute time tag in days:hours:mins:secs

00:00:00:09.0000: 00,03,08,29,31<CR><LF>

FMTANA HEXS,N,CM,ABS,DHMS<TM> ASCII hex with spaces / cumulative / absolute time tag in days:hours:mins:secs

00:00:00:09.0000: A0 00 01 09<CR><LF>

FMTANA IND,N,CM,ABS,MSEC<TM> individual / cumulative / absolute time tag in tenths of milliseconds

9000.0: 00,03,08,29,31<CR><LF>

FMTANA IND,N,EV,ABS,DATE<TM> individual / by event / absolute time tag / date format

07/20/91 13:05:10.0000: 08<CR><LF>
07/20/91 13:05:18.1090: 29,31<CR><LF>
07/20/91 13:05:18.1230: 00<CR><LF>
07/20/91 13:05:18.2230: 03<CR><LF>
NO ENTRIES<CR><LF>

FMTANA BIN,N,EV,ABS,BIN4<TM> binary / by events / absolute time tag / in 4-byte binary

<00><01><5F><90><00><00><01><00><CR><LF>
<00><02><9C><52><0A><00><00><00><CR><LF>
<00><02><9C><DE><00><00><00><01><CR><LF>
<00><02><A1><2A><00><00><00><08><CR><LF>
NO ENTRIES<CR><LF>

FMTANA BIN,N,EV,ABS,BIN8<TM> binary / by events / absolute time tag / in 8-byte binary

<00><00><00><00><00><01><5F><90><00><00><01><00><CR><LF>
<00><00><00><00><00><02><9C><52><0A><00><00><00><CR><LF>
<00><00><00><00><00><02><9C><DE><00><00><00><01><CR><LF>
<00><00><00><00><00><02><A1><2A><00><00><00><08><CR><LF>
NO ENTRIES<CR><LF>

Command: FMTDIG (Format of Digital Data)

Syntax: FMTDIG [A],[B]<TM>
or FD [A],[B]<TM>

Mode: Analog or Digital

Purpose: This defines the format of the data returned by the DATA? command in Digital mode.

Description: [A] defines the format for the returned data:

[A]	Data returned in
HEXA	in 8-digit ASCII hexadecimal (4-digit ASCII hexadecimal in Combination Analog/Digital mode)
HEXS	in 8-digit ASCII hexadecimal with spaces between every two digits (4-digit ASCII hexadecimal in Combination Analog/Digital mode)
BIN	in 32-bit binary (16-bit in Combination Analog/Digital mode)
BINN	in 32-bit binary (16-bit in Combination Analog/Digital mode). <CR><LF> is not returned in this case. The END bit will be asserted with the last byte of binary data.
BINC	in 32-bit binary (16-bit in Combination Analog/Digital mode). A space character is included before the binary data.
BINNC	in 32-bit binary (16-bit in Combination Analog/Digital mode). A space character is included before the binary data, and <CR><LF> is not returned in this case. The END bit will be asserted with the last byte of binary data.
BINA	in 32-bit ASCII binary (16-bit in Combination Analog/Digital mode)
BINS	in 32-bit ASCII binary with spaces between every eight digits (16-bit in Combination Analog/Digital mode)
BINF	in 32-bit binary. This is a special format which connects the VXI interface directly to the instrument hardware (digital input latches or front connector inputs), allowing this module to be read back at rates greater than 100 KHz (assuming the controller is quick enough). However, this format is only supported in full Digital mode, and returns the channels as bit-mapped in hardware, which is a different bit mapping than the other formats listed here. The bit format is listed below.

[B] an optional parameter which defines the source of the data:

[B]	Source
LAT	digital input latches. All channels disabled with the ENB command will be returned as a 0.
IN	digital inputs, ahead of the digital input latches. The state of the inputs will be returned independent of which channels are enabled with the ENB command.

If [B] is omitted, the source of the data will remain as last programmed.

The data in all formats except BINF is returned with the most significant bit (leftmost) being channel 31 and the least significant bit (rightmost) being channel 0 (or channel 16 in Combination Analog/Digital mode). The bit positions in BINF are that of the hardware, as shown below, from most significant (left) to least significant (right):

Channels 19, 18, 17, 16, 3, 2, 1, 0, 23, 22, 21, 20, 7, 6, 5, 4, 27, 26, 25, 24, 11, 10, 9, 8, 31, 30, 29, 28, 15, 14, 13, 12.

The default setting is FMTDIG HEXA,LAT.

Example: Following are examples of what the response data to the DATA? or DATA? R command would be according to the given FMTDIG command.

Assume bits 31, 29, 8, 3, and 0 were in the active state at strobe time, and all other bits were in the inactive state.

FMTDIG BIN<TM> binary (the four character binary representation is represented here by four hex values within brackets < >)
<A0><00><01><09><CR><LF>

FMTDIG BINA<TM> ASCII binary with spaces
10100000000000000000000100001001<CR><LF>

FMTDIG BINS<TM> ASCII binary with spaces
10100000 00000000 00000001 00001001<CR><LF>

FMTDIG HEXA<TM> ASCII hex
A0000109<CR><LF>

FMTDIG HEXS<TM> ASCII hex with spaces
A0 00 01 09<CR><LF>

FMTDIG BINN<TM>
<A0><00><01><09>

FMTDIG BINC<TM>
<20><A0><00><01><09><CR><LF>

FMTDIG BINNC<TM>
<20><A0><00><01><09>

FMTDIG BINF<TM>
<09><00><01><A0>

Command: HYST (Programmable Hysteresis)

Syntax: HYST [A]<TM>
or H [A]<TM>

Mode: Analog

Purpose: Turns programmable hysteresis on and off.

Description: [A] is either ON or OFF:
ON programmable hysteresis on
OFF programmable hysteresis off

Programmable hysteresis allows two voltages to be defined (by the TRG command), such that the input signal should only be recorded when it exceeds the higher of the two values, and not recorded again until it goes below the lower of the two values, and not again until it exceeds the higher value, and so forth. Any channel that is to be continually captured should also have its Flip bit set.

When switching from programmable hysteresis OFF to ON, all dual voltages previously defined with the TRG command will become active. When switching from ON to OFF, each channel will take on the average of any dual voltage given with the TRG command. When switching from ON to OFF or OFF to ON, the Event buffer will be cleared.

Note that the time uncertainty is different depending on whether programmable hysteresis is on or off.

For further details, refer to the TRG command.

Example: HYST ON<TM> programmable hysteresis is now on, all dual voltages previously defined with the TRG command will become active, and the Event buffer is cleared.

Command: INT (Interrupt Enable)

Syntax: INT [A]<TM>

Mode: Analog or Digital

Purpose: This command enables generation of the VXIbus Request True interrupts.

Description: The INT command enables generation of VXIbus Request True interrupts. Interrupts occur either when the equation sent with the EQU command becomes true (EQU), or when an error occurs (ERR).

The [A] parameter can take one of two forms. If [A] is sent as a number, it is as follows:

[A]	Specifies
1	EQU interrupt enabled
2	ERR interrupt enabled
3	both EQU and ERR interrupts enabled

[A] may also be sent as the string EQU and/or ERR, defining which interrupt to enable. To enable both interrupts, use a comma to separate the two terms (see the third example below). Upon enabling, any pending interrupts will cause an interrupt to occur.

For further information on interrupts which occur due to their voltage states, refer to the EQU command. For further information on programming errors, refer to the ERR? command.

Example:

INT EQU<TM>	EQU interrupts are enabled.
INT ERR<TM>	ERR interrupts are enabled.
INT EQU,ERR<TM>	Both EQU and ERR interrupts are enabled.
INT 1<TM>	EQU interrupts are enabled.
INT 3<TM>	Both EQU and ERR interrupts are enabled.

Command: INT? (Interrupt Query)

Syntax: INT?<TM>
or I?<TM>

Mode: Analog or Digital

Purpose: Returns the bottom four bits on the VXI status register, which denotes the state of the VXIbus Request True interrupt.

Description: There are two reasons for a Request True interrupt: 1) programming error, or 2) the equation defined by the EQU command becomes active. If a programming error interrupt is pending, bit 1 is 1; otherwise it is 0. If the equation interrupt is pending, bit 0 is 1; otherwise it is 0. These bits are set whether or not interrupts are enabled. They are cleared by a Read STB command (which occurs during a serial poll in IEEE-488 systems) or by the INT2? command. The response is formatted as a 1-character ASCII hex digit followed by a <CR><LF>.

The system controller is not required to read all three characters of response data. It may read any number from one to three characters.

This command does not reset the interrupt condition (and bits 0 and 1). To reset the interrupt condition use a Read STB command (which is executed on a 488 serial poll in IEEE-488 systems) or an INT2? command.

Example: INT?<TM>

Response data of:
1<CR><LF>
indicates the equation defined by the EQU command has been satisfied.

Response data of:
3<CR><LF>
indicates that the equation defined by the EQU command has been satisfied and a programming error has occurred.

Command: INT2? (Interrupt Query)

Syntax: INT2?
or I2?

Mode: Analog or Digital

Purpose: Returns the bottom four bits of the VXI status register, which defines the state of a VXIbus Request True interrupt.

Description: This command is identical to the INT? command except it resets the interrupt condition (and bits 6, 1, and 0 of the Status register) every time it is executed. An optional method of resetting the interrupt condition is to use the Read STB system command (which is executed on a 488 serial poll in IEEE-488 systems).

The Read STB is generally preferred when using interrupts. For example, when this module's commander is an IEEE-488 interface device, a serial poll (which causes a Read STB) must be issued before the IEEE-488 interface device removes its SRQ (service request) line.

Example: INT2?
Response data of:
1<CR><LF>
indicates the equation defined by the EQU command has been satisfied.

If INT2? is immediately executed again, and the EQU command did not again become satisfied since the last time it was read, the response would be:
0<CR><LF>

Command: IST (Internal Self Test)

Syntax: IST<TM>

Mode: Analog or Digital

Purpose: To initiate a self test.

Description: The self test consists of six separate tests. During power-up or reset all six tests are performed, and during the IST command, all tests except for the RAM and NOVRAM tests are performed. During the power-up or reset self test, the name of the test being performed is displayed on the front panel LEDs. Any test that fails will cause the test name to flash on the display.

The tests, in the order they are executed, are as follows. The test name shown on the front panel display is in parentheses.

Test 1: RAM test (RAM)
All onboard RAM is tested, first with a pattern of 55 hex, then a pattern aa hex, and then a walking 1s pattern. If this test fails, the module will be unable to function properly after it flashes the RAM error on the front display.

Test 2: Nonvolatile RAM (NRAM)
This tests the onboard nonvolatile RAM which holds the calibration data. If this has completely failed, it will queue up "11,INOPERATIONAL NOVRAM". If nonvolatile RAM is operational but the data in it is corrupt (returns an illegal block check), a "12,NOVRAM BLOCK CHECK ERROR" will occur. If the block check error occurs, the NOVRAM will be programmed with default calibration data. The next time the module is reset, the block check error should not occur (but a "10,UNCALIBRATED CHANNELS: 0-31" error should).

Test 3: Slave Microprocessor (µPRC)
This test validates the operation of the onboard slave microprocessor, which is responsible for programming the FPGAs (Field Programmable Gate Arrays), updating channel thresholds and keeping the time tag. If this test fails, the VXI interface will still function, but all channels will be nonfunctional. The error "13,INOPERATIONAL SLAVE MICROPROCESSOR" will be queued up.

Test 4: Field Programmable Gate Array (FPGA)
This test will not be executed if Test 3 failed. The FPGA test checks the two onboard field programmable gate arrays. If they are not operating properly the error "14,FPGA WILL NOT PROGRAM CORRECTLY" will be queued up.

Test 5: Inputs (INPS)
This test will not be executed if either the Slave Microprocessor (Test 3) or FPGA test (Test 4) failed.

All 32 inputs are relay isolated, and an onboard voltage source will be switched in. The channels are tested at +12V, +6V, 0V, -6V, and -12V, and any channel not within 5% of the tested voltage will be considered in error. The +6V, 0V, and -6V tests are performed in the ±10V range, and the +12V and -12V tests are performed in the ±50V range.

Up to five errors may be queued up with this test (one for each voltage). For the +12V test, the queued error will be "15,CHANNELS FAILED +12V TEST:

[CHANNELS]". [CHANNELS] specifies all channels not passing. Any three or more consecutive channels will have the first and last channel separated by a dash, and all other channels will be separated by commas. An example would be 15,CHANNELS FAILED +12V TEST: 0,2-4,6,7,23. Any channels failing the other tests will similarly have an error message queued up.

Test 6: Calibration test (CAL)
This test checks to see if the calibration data is valid for each channel. If all channels have not previously been calibrated, or the onboard nonvolatile RAM containing the calibration data has failed, the error message "10,UNCALIBRATED CHANNELS: [CHANNELS]" is queued up. (See the ERR? command for a full description of this message.) All uncalibrated channels will still operate correctly, but their accuracy could be off as much as 5%. [CHANNEL] has the same syntax as listed under the Inputs test above.

In Digital mode, the digital input latches will be cleared at the end of self test. In Analog mode, all comparator status latches will, likewise, be cleared at the end of self test. All other setup, in both modes, reverts to the state it had before self test was initiated.

Example: IST<TM>

Possible response data upon errors:
15,CHANNELS FAILED +12V TEST: 2,23-25,27,29<CR><LF>
15,CHANNELS FAILED +6V TEST: 23-25<CR><LF>
10,UNCALIBRATED CHANNELS: 0-4<CR><LF>
00,NO ADDITIONAL ERRORS TO REPORT<CR><LF>

Response data upon no errors:
00,NO ADDITIONAL ERRORS TO REPORT<CR><LF>

Command: NAME (Name)

Syntax: NAME [C],[N]<TM>
or N [C],[N]<TM>

Mode: Analog

Purpose: This command is used to give a name to a channel to be displayed on the front panel.

Description:

[C] a 1- to 2-digit channel number from 0 to 31 which specifies the channel to be named.

[N] a 4-character name, which will be right justified on the display. If some of the characters are spaces, the name should be enclosed by quotation marks, either single or double. If quotation marks are part of the name, and are the same type (single or double) as the enclosing quotation marks, they may be specified by doubling them. For example, "1""2" would result in the name 1"2. '1""2' would result in the name 1""2. This string follows the IEEE 488.2 rules for <STRING PROGRAM DATA>.

In Analog mode, channels that are on the "wrong" side of their respective threshold are displayed on the front panel display. The default is CH00 for channel 0, CH01, for channel 1, and so forth. This command allows these channels to be renamed to any 4-character name.

Example:

NAME 0,' S1'<TM>	Channel 0 is now named 'S1'. The quotation marks ensure that S1 will be centered in the display.
NAME 1,PS12<TM>	Channel 1 is now named 'PS12'.
NAME 2,+12V<TM>	Channel 2 is now named '+12V'.
NAME 03,' -5V'<TM>	Channel 3 is now named ' -5V'. A leading space will appear on the display whether or not the quotation marks are present, since the name is right justified.

Command: OUTPUT

Syntax: OUTPUT [A]<TM>
or O [A]<TM>

Mode: Analog or Digital

Purpose: Enables TTL outputs.

Description: [A] is either ON or OFF:

ON	TTL outputs not tri-stated
OFF	All TTL outputs tri-stated

The default condition is all TTL outputs tri-stated.

Command: REENB (Analog Channel Re-enable)

Syntax: REENB [F],[E],[Q],[CHANNEL STRING]<TM>
or R [F],[E],[Q],[CHANNEL STRING]<TM>

Mode: Analog

Purpose: Re-enables selected channels when in Analog mode.

Description: [CHANNEL STRING] is a multicharacter string defining which channels are to be re-enabled. [CHANNEL STRING] has the format:

[CHANNEL],[CHANNEL],...[CHANNEL]

where [CHANNEL] is:
a channel number between 0 and 31, or
a range of channels in the form:
<number 0 to 31> TO <number 0 to 31>

There may be any number of white spaces (including zero) before and after any TO.

This command re-enables a channel previously enabled with the EQU command. All channels returned via the DATA? command (with the exception of those having their Flip bits set) must be re-enabled if they are to be recorded again and cause another interrupt. If DATA? R is used when reading returned data, the channels are automatically re-enabled, and this command does not have to be used.

[F] (for 'force') is optional and defines whether to force re-enabling of all specified channels. If [F] is omitted, only the specified channels that are not residing in the Event buffer will be re-enabled. This is the normal use, and guarantees that multiple entries of the same channel do not exist in the Event buffer at the same time (unless of course the Flip Continuous bit on a channel is set). If [F] is specified, all specified channels are re-enabled independent of whether or not they exist in the Event buffer, (which does not guarantee only one entry of a channel exists in the buffer at a time, since a transition can occur between the time the last entry is read from the Event buffer and the time this command is sent).

[E] (for 'Event buffer clear') is optional and if given clears the Event buffer before executing the REENB command as if a RST EVNT;REENB command sequence were given. The difference is that the [E] option guarantees that no channels are recorded between the Event buffer clearing and the re-enabling process (refer to Appendix D for further details).

[Q] (for 'eQuation period reset') is optional. If given, it clears the equation period before executing the REENB command as if a EQURST;REENB command sequence were given. The difference is that the [Q] option guarantees that no channels are recorded between when the equation is cleared and the re-enabling process (refer to Appendix D for further details).

Note that in any instance where the REENB command is sent, the EQU command can be used in its place, since they both enable Analog channels. The difference in these two commands is that the REENB command only affects channels that

already have been specified in the EQU command, it does not effect the present Boolean equation, it can only enable channels, and it operates much faster. Unlike the REENB command, the execution time of the EQU command is proportional to the number of entries presently in the Event buffer.

Refer to the command descriptions of the EQU, DATA?, DATA? R and REENB commands.

Example: REENB<TM> Re-enable all channels not already in the Event buffer.

Command: REV? (Revision Level)

Syntax: REV?<TM>

Mode: Analog or Digital

Purpose: The REV? command instructs the module to return the revision level of the onboard microprocessor firmware.

Description: This command returns the revision level of the onboard firmware as an alphanumeric string representing the revision level.

Example: REV?<TM>

An example of a typical response is:

REVISION 1.0<CR><LF>

Command: RST (Reset Module)

Syntax: RST [A_1],[A_2], ... [A_n]<TM>

Mode: Analog or Digital

Purpose: The RST command resets specified portions of the module to the power-up state.

Description: If no options are specified, all of the following listed under the [A] option are performed.

If options are specified, only the specified portions of this module are reset to the power-up condition. Any option may be abbreviated by using its first two characters. [A] may be any of the following:

[A]	Effects (Power-up state)
AD	Mode - Analog mode
APER	Aperture time - 10 milliseconds
ARM	Module unarmed
DEB	Debounce counter time - 1/10 of a second Debounce enable - all channels disabled
DISP	Analog channel priority - 0 highest, 31 lowest Analog display mode - real time Digital display mode - real time Digital display byte order - 1, 0, left to right
EPOL	Polarity of EQU OUT signal - active low
EQU	Inputs when in Analog mode - disabled Comparator status latches - cleared
ENB	Inputs when in Digital mode - enabled
ERR	Error buffer - cleared Error LED - off
EVNT	Event buffer (buffer holding all occurrences of any channel being on "wrong" side of its threshold) - cleared. If this module is armed, and the ARM option is not also given, then more entries may immediately be collected.
FLIP	Flip bits - cleared (both sets)
FMT	Analog readback format - returned by individual channel number with polarity and transition information included, by event, relative time tag in seconds (FMTANA, IND,PL,EV,REL,SEC). Abbreviated mode (ABREV) is reset. Digital readback format - returned in ASCII hex (FMTDIG HEXA,LAT), from digital input latches
HYST	Programmable hysteresis - off
INT	Interrupts disabled
NAMES	Channel names = CH<channel number> where <channel number> is a two digit number.
OUTENB	TTL Outputs - tri-stated
RTYPE	Readback type - errors
STB	External strobe - Disabled, strobe on readback of digital data
SYNC	Source of counter synchronization pulse - P4
TIME	Current time - zeroed

	VHYST	Voltage hysteresis compensation (performed during voltage commands) - disabled
	VOLT	Threshold level - 1.4V Range - ±10 volt range Trigger sense - Greater than threshold level (>)

Example:

RST<TM>	The module is reset to the power-up state.
RST ERR,EVNT<TM>	Error buffer and Event buffer are both cleared. Nothing else is changed.

Command: RSTX (Reset Module Except)

Syntax: RSTX [A_1],[A_2], ... [A_n]<TM>

Mode: Analog or Digital

Purpose: The RSTX command resets all EXCEPT the specified portions of the module to its power-up state.

Description: The options for [A] are listed in the RST command. If no options are specified, the entire module is reset to its power-up state.

Example:

RSTX<TM>	Module is reset to the power-up state.
RSTX ERR<TM>	The entire module is reset to power-up state except for the Error buffer.

Command: SET (Set Time Tag Counter)

Syntax:
SET [A],[B],[C]<TM>
or STT [C]<TM> SET TIME
or STD [C]<TM> SET DATE
or STS [C]<TM> SET SEC
or SST [C]<TM> SET SYNC TIME
or SSS [C]<TM> SET SYNC SEC

Mode: Analog or Digital

Purpose: The SET command programs the time used for time tagging.

Description: All time tags returned with the next DATA? or DATA? R command will be with reference to the time specified by this command, including entries in the Event buffer which existed before this command was received.

[A] an optional parameter, the string SYNC. If specified, the time value given will be updated when a SYNC pulse is received. The resynchronized time will take effect with the next DATA? command. Any SYNC pulse between 1 second before the SET SYNC command is received until a SYNCOFF command is received will update the current time to the given value. The 1 second period allows some flexibility in the timing relationship between the sync pulse and the sending of this command. If [A] is omitted, the current time will be updated immediately upon receiving the command.

[B] defines the format of the time sent, and [C] is the actual time sent. [B] and [C] may have the following values:

[B]	Description
SEC	[C] represents the time in seconds. It may be in the range 0.0000 to 429,496.7295 seconds.
TIME	[C] is a string representing the time of day, in the form: <hours>:<minutes>:<seconds> where <hours> is any valid integer number from 0 to 23. <minutes> is any valid integer number from 0 to 59, and <seconds> is any valid number between 0.0000 and 59.9999
DATE	[C] is the string representing the date, in the form: <month>/<day>/<year> where <month> is any valid integer number from 1 to 12 <day> is any valid integer number from 1 to 31 <days> is are any valid integer number representing the year.

If [B] = SEC, the given value specifies the absolute time of this module. This is used with the SEC, MSEC, DHMS options of the format command (FMTANA). If [B] = DATE or TIME, the combination of the date and time values specify the

absolute time of this module. This is used with the DATE option of the format command.

Note that the SET SYNC,TIME command sets the time of day to its specified value upon a SYNC signal.

On reset, the module takes on a date of 1/1/80 and a time of 00:00:00, for TIME/DATE option and 0 secs for the SEC option.

Examples:

SET SEC,5445<TM>	The current time is set to 5445 seconds.
SET DATE,7/20/90<TM>	The current date is set to July 20, 1990.
SET TIME,20:02:04.1234<TM>	The current time is set to 8:02PM (and 4.1234 seconds)
SET SYNC,SEC,0<TM>	The next SYNC pulse will reset the current time to 0.
SET SYNC,TIME,20:02:04<TM>	The next SYNC pulse will set the time of day to 8:02PM (and four seconds)
SSS 0<TM>	Same as SET SYNC,SEC,0<TM>

Command: STB (Strobe)

Syntax: STB [A]<TM>
or S [A]<TM>

Mode: Digital

Purpose: The Strobe command specifies when to latch into the digital input latches the data present on the digital input lines.

Description: When the strobe signal occurs, all data is simultaneously latched into the digital input latches. [A] defines the source of the strobe signal. Data is latched in on a leading edge of the strobe signal.

[A]	Strobe signal is taken from:
0	VXI TTLTRG* 0
1	VXI TTLTRG* 1
2	VXI TTLTRG* 2
3	VXI TTLTRG* 3
4	VXI TTLTRG* 4
5	VXI TTLTRG* 5
6	VXI TTLTRG* 6
7	VXI TTLTRG* 7
±8	Front Panel
OFF or 9	No source
RD or 10	No external trigger. Data is latched each time input is requested by the system controller from this module.
S or 11	Software Trigger. Data is latched with the reception of this command.

If [A] = 0 to 7, data will be captured upon receiving a pulse on the appropriate VXI trigger line (assuming the Counter Sync signal does not have control of the TTLTRG* lines via a SYNC 0-7 command). The polarity is active low, complying with the VXIbus defined Synchronous Trigger Protocol.

If [A] = ±8, data will be captured upon receiving a pulse on the front panel STB/ARM connector. The polarity of the pulse is defined by whether [A] is positive (active high) or negative (active low).

The default is STB RD (no external trigger), latch data on readback.

Example:

STB 2<TM>	Using TTLTRG* 2 (if the SYNC 0-7 command has not been given)
STB -8<TM>	Using Front Panel strobe, active low polarity
STB OFF<TM>	Disabled Strobe
STB RD<TM>	Strobe on readback

Software Trigger (3 examples). Note that the white space is optional before parameter [A] in this command:

STB S<TM>
S S<TM>

Command: SYNC (Synchronize Time Tag Counter)

Syntax: SYNC [A]<TM>
or SY [A]<TM>

Mode: Analog or Digital

Purpose: Specifies which signal synchronizes the time tag counter.

Description: [A] must be one of the following:

[A]	Synchronization signal is taken from
0	VXI TTLTRG* 0
1	VXI TTLTRG* 1
2	VXI TTLTRG* 2
3	VXI TTLTRG* 3
4	VXI TTLTRG* 4
5	VXI TTLTRG* 5
6	VXI TTLTRG* 6
7	VXI TTLTRG* 7
±8	Front Panel

Counter synchronization is enabled when a SET SYNC command (which defines the synchronization time) is received, and disabled when a SYNCOFF command is received. Within this time period, any pulse occurring on the line specified by [A] will resynchronize the time tag counter. The resynchronized time will take effect with the next DATA? command.

If [A] = 0 to 7, the time tag counter is synchronized by a pulse on the appropriate VXI trigger line. The polarity is active low, complying with the VXIbus defined Synchronous Trigger Protocol. If a TTLTRG* line was previously specified for the Arm or Strobe signal (with the ARM or STB command), it will be disconnected from the Arm or Strobe function.

If [A] = ±8, the time tag counter is synchronized by a pulse on the Counter Sync line of P4 of the front panel. The polarity of the pulse is defined by whether [A] is positive (active high) or negative (active low). If a TTLTRG* line was previously specified for the Arm or Strobe signal (with the ARM or STB command), it will be reconnected to the Arm or Strobe Function.

Counter synchronization is enabled 1 second before the SET SYNC command is received by this module. The 1 second period allows some flexibility in the timing relationship between the pulse and the sending of the SET SYNC command.

Example: SYNC 2<TM> Uses TTLTRG* 2.

SYNC -8<TM> Uses Front Panel Counter Sync signal, active high polarity

Command: SYNC? (Sync Query)

Syntax: SYNC?<TM>
or SY?<TM>

Mode: Analog

Purpose: Returns whether or not a SYNC signal has come in.

Description: This command may be used after sending a SET SYNC command, to determine if the sync signal has been received. A SYNC signal may come in any time after 1 second before the SET SYNC command is received by this module. The 1 second period allows some flexibility in the timing relationship between the sync pulse and the sending of this command.

One of three different responses will be returned:

0,SYNC NOT RECEIVED<CR><LF>
The sync signal has not been received.

1,SYNC RECEIVED<CR><LF>
The sync signal has been received.

2,SET SYNC COMMAND NEVER RECEIVED OR INACTIVE<CR><LF>
Either the SET SYNC command was never received or a SYNCOFF command has been received since the last SET SYNC command was sent.

For quicker overall performance time, the complete message does not have to be read (the first digit holds all information). Sending any command after reading any portion of the response message will cause the remaining portion of the message to be taken out of the output buffer.

Example: SET SYNC,SEC,0<TM>
SYNC?<TM>
1,SYNC RECEIVED<CR><LF>

Command: SYNCOFF (Synchronize Time Tag Counter Off)

Syntax: SYNCOFF<TM>
or SO<TM>

Mode: Analog

Purpose: Disabled SYNC signal.

Description: This command is usually used after a SET SYNC command to disable the SYNC input. Any SYNC signal coming between 1 second before the SET SYNC command and up to the reception of the SYNCOFF command will update the current time of the module to that specified by the SET SYNC command.

Example: SYNCOFF<TM>

Command: TRG (Trigger)

Syntax: TRG [TRIGDEF]<TM>
or T [TRIGDEF]<TM>

Mode: Analog or Digital

Purpose: Programs the voltage level threshold and the logic sense or trigger condition of each channel.

Description: The TRG command is used to program the voltage level threshold of each channel and the logic sense or trigger condition of each channel. This command automatically selects the most sensitive range consistent with the programmed threshold voltage level.

[TRIGDEF] is a multicharacter string defining the channel number, threshold level and trigger sense. [TRIGDEF] has the format:

[CHANNEL STRING][POL][THRESHDEF]

[CHANNEL STRING] is a multicharacter string defining which channels the command applies to. It has the format:

[CHANNEL],[CHANNEL],...[CHANNEL]

where [CHANNEL] is:

a channel number between 0 and 31, or
a range of channels in the form:
<number 0 to 31> TO <number 0 to 31>

There may be any number of white spaces (including zero) before and after any TO. White spaces may exist between [CHANNEL STRING] [POL] or [THRESHDEF]. The leftmost channel has the highest priority.

If [CHANNEL STRING] is omitted, this command applies to all channels as if [CHANNEL STRING] were 0 TO 31.

[POL] is either < or >. the meaning of these characters depends on whether the module is in Digital or Analog mode:

Digital mode:	>	active high logic
	<	active low logic
Analog mode:	>	indicates that the input voltage must exceed the programmed threshold voltage to set an individual comparator status latch and be recorded.
	<	indicates that the input voltage must go below the programmed threshold voltage to set an individual comparator status latch and be recorded.

[THRESHDEF] defines the threshold and takes one of two forms. If a single value is given for [THRESHDEF], this value represents the threshold voltage. If two values separated by a comma are given here (and programmable hysteresis is active [HYST command]), the first value defines the threshold below which the input signal must go to cause this channel to be recorded, and the second defines the threshold that a signal must exceed in order to be recorded.

That is, if [POL] = <, the first threshold is active. If [POL] = >, the second threshold is active. If this channel has the Flip bit enabled, when it flips, the applicable threshold also changes.

If programmable hysteresis is not active when two values are given, the single threshold for this channel is programmed to the average of these two values.

It is important to note that if two values are given (and programmable hysteresis is active), the two values define a voltage hysteresis, and not a band of voltage detection. The following example illustrates the difference.

Assume the two given values are +2V and +6V, the signal is at 4V, and the flip state is initially negative (<). The signal can then transition about the 6V threshold but it will not be recorded because the signal has not yet gone below the lower hysteresis value. Once it does go below 2V it will be recorded once, and then may transition about the 2V level without being recorded. If it again exceeds 6 volts, it will again be recorded.

A band of voltage detection (where a signal is recorded every time it goes above or below two voltage thresholds) can be obtained by connecting a signal to two channels, and defining one channel to have a positive (+) trigger sense and the other channel to have a negative (-) trigger sense. The Flip bit in this case would not be set.

If the programmed threshold falls within the ±10 V, the most sensitive range is selected. Otherwise the ±50 V range applies.

Examples: Digital Mode

TRG 0TO31>1.5<TM>	all channels are active high. A 1 is returned if the input voltage exceeds 1.5V, a 0 if it is below.
TRG 31 TO 0< 1.5<TM>	all channels are active low. A 1 is returned if the input voltage is below 1.5V, a 0 if it is above.
TRG 2 < -2.01<TM>	Channel 2 is active low. A 1 is returned if the input voltage is below -2.01V, a 0 if it is above.

Analog Mode

Assume that the equation EQU 0 TO 31 < TM > was sent previous to this Trigger command, individually enabling all channels. (This is also the default condition.)

TRG 0TO31 < 1.5 < TM > — Information will be recorded, and an interrupt generated on any channel that has a voltage level on it below 1.5V.

TRG 31 TO 0 > 1.5 < TM > — Information will be recorded, and an interrupt generated on any channel that has a voltage level on it above 1.5V.

TRG 2,5TO6 < -2.01,4.2 < TM >

If programmable hysteresis is enabled (HYST command), information will be recorded, and an interrupt generated if channel 2, 5, or 6 has a voltage of less than -2.01V. If the Flip bit of the appropriate channel is set, the channel will be recorded again (and another interrupt will occur) if after it goes below -2.01V, it then exceeds 4.2V.

If programmable hysteresis is not enabled, information will be recorded, and an interrupt generated if channel 2, 5, or 6 has a voltage of less than 1.095V (average of -2.01 and 4.2).

Assume that the EQU 1 + 2 * 30 < TM > was sent previous to this trigger command.

TRG 0 TO 31 < 1.5 < TM > — Information will be recorded and an interrupt generated if channels 1, 2, or 30 go below 1.5V.

Command: TRGH (Trigger High Range)

Syntax: TRGH [TRIGDEF]<TM>
or TH [TRIGDEF]<TM>

Mode: Analog or Digital

Purpose: Programs the voltage level threshold and logic sense or trigger condition of each channel, within the ±50V range.

Description: This command operates identical to the TRG command, except that it forces the use of the high, less sensitive ±50V range.

Example: TRGH 0 TO 31<1.5<TM> Information will be recorded, and an interrupt generated on any channel that has a voltage level on it below 1.5V.

Command: TRGL (Trigger Low Range)

Syntax: TRGL [TRIGDEF] < TM >
or TL [TRIGDEF] < TM >

Mode: Analog or Digital

Purpose: Programs the voltage level threshold and logic sense or trigger condition of each channel, within the ± 10V range.

Description: This command operates identical to the TRG command, except that it forces the use of the low, more sensitive ± 10V range.

Example: TRGL 0 TO 31 < 1.5 < TM > Information will be recorded, and an interrupt generated on any channel that has a voltage level on it below 1.5V.

Command: VHYST (Voltage Hysteresis Compensation Enable/Disable)

Syntax: VHYST [A]<TM>

Mode: Analog or Digital

Purpose: Turns on/off th tage compensation performed during voltage commands.

Description: [A] must be one of the following:

[A]	Action
ON	voltage hysteresis compensation will be performed during voltage commands.
OFF	voltage hysteresis compensation will not be performed during voltage commands

There is a fixed hysteresis of 15 millivolts on each channel input, which is compensated for when taking a voltage reading (VOLT?, VOLTL?, VOLTALL?, VOLTALLL?) in order to obtain the most accurate reading. This hysteresis compensation takes place only when taking a voltage measurement within the ±10 volt range. An improvement in reading speed, however, can be obtained if this compensation is turned off, which results in decrease in accuracy of approximately 7 millivolts. Speed savings under different conditions are given in Appendix E, Voltage Measurement on the VX4286.

Command: VOLT? (Volt Query)

Syntax: VOLT? [L],[B]<TM>
or V? [L],[B]<TM>

Mode: Analog or Digital

Purpose: This command returns the DC voltage of the input channel.

Description: The VOLT? command returns the maximum and minimum voltage, and the average of the maximum and minimum voltage on the specified channel [B]. [B] can be a 1- to 2-digit number specifying channel 0 to 31. The module will automatically select the most sensitive range depending on whether or not the input is within ±10V.

Parameter [L] is optional and defines whether labels should be included in the returned value. If [L] is specified, the returned values will be in one of the following two formats, depending on whether the VOLTFULL or VOLTAVE command is active. If VOLTFULL is active, the returned values will have the format:

AVE = <ave value>, MIN = <min value>, MAX = <max value><CR><LF>

If VOLTAVE is active, the returned values will have the format:

AVE = <ave value><CR><LF>

If [L] is omitted, the returned values will be in the format:
<ave value>, <min value>, <max value> (VOLTFULL active)
or <ave value> (VOLTAVE active)

The returned values will be the maximum, minimum (and the average of these two) voltages during the measurement time.

The format of the response data is:
±xx.xxx<CR><LF>
where x is a decimal digit between 0 and 9. The leading x will not be sent if the value is between 9.999 and -9.999 volts (no leading zeroes).

The module first attempts the measurement within the ±10V range. If the voltage is not within this range, it then takes a measurement within the ±50V range. If the voltage is also outside the ±50V range, a VOLTAGE OVERFLOW or VOLTAGE UNDERFLOW message will be returned.

As with all DC voltmeters, the DC accuracy depends on the aperture time of the measurement device (APER command) and the repetition rate of the input signal. For full accuracy, the input signal must be a repeatable waveform (a DC signal can be seen as repeatable at a repetition period of 0), and the repetition period must be less than the programmed aperture time. (This module will return the result of a nonrepeatable, random signal [or where the repetition period is greater than the aperture time], as the DC voltage of the waveform at some particular point of time during the measurement interval.) A complete description of the voltage measurement is given in Appendix E.

If the module was in Analog mode during this command, any transitions to the "wrong" side of the threshold on this channel will not have been detected. If in Digital mode, the particular bit corresponding to this channel will be cleared. The TTL output of this channel may transition while this command is in operation. Operations on all other channels are not affected.

If debounce is enabled on this channel, an accurate voltage reading will only be made if the debounce time is much less than the aperture time. Also in this situation, any voltage maximums or minimums that are shorter than the debounce time will be filtered out. Any time a voltage reading is taken on a channel with debounce enabled, the warning "22,VOLT COMMAND MAY NOT WORK WITH DEBOUNCE ENABLED" will be queued in the Error buffer.

Examples: If channel 1 has 9.634 volts on its input with 0.030 volts peak-to-peak of AC, the command:

VOLT? 1<TM>

will return

+9.634, +9.519, -9.664<CR><LF>

If channel 31 has a 10V square wave centered about 0 volts, the command:

VOLT? L,31<TM>

will return

AVE = 0.000, MIN = -5.000, MAX = +5.000<CR><LF>

Command: VOLTALL? (Voltage Query, All Channels)

Syntax: VOLTALL? [L],[CHANNEL STRING]
or VA? [L],[CHANNEL STRING]

Mode: Analog or Digital

Purpose: Takes a voltage measurement on all channels simultaneously.

Description: Parameter [L] is optional and defines whether labels should be included in the returned value. If [L] is specified, the returned values will be in one of the following two formats, depending on whether the VOLTFULL or VOLTAVE command is active. If VOLTFULL is active, the returned values will have the format:

AVE = <ave value>, MIN = <min value>, MAX = <max value><CR><LF>

If VOLTAVE is active, the returned values will have the format:

AVE = <ave value><CR><LF>

If [L] is omitted, the returned values will be in the format:
<ave value>, <min value>, <max value> (VOLTFULL active)
or <ave value> (VOLTAVE active)

[CHANNEL STRING] is a multicharacter string defining which channels are to have their voltage returned. [CHANNEL STRING] has the format:
[CHANNEL],[CHANNEL],...[CHANNEL]

where [CHANNEL] is:
a channel number between 0 and 31, or
a range of channels in the form:
<number 0 to 31> TO <number 0 to 31>

There may be any number of white spaces (including zero) before and after any TO.

This command checks both the ±10V and the ±50V range, as described in the VOLT? command. One voltage message will be returned for each channel specified in the [CHANNEL STRING], in the order given. The voltage measurement and syntax of the returned message is identical to that shown in the VOLT? command. A complete description of the voltage measurement is given in Appendix E.

Example:

VOLTFULL<TM>
VOLTALL? L,0 TO 2<TM>

This will return

AVE = 2.034, MIN = 2.034, MAX = 2.034<CR><LF>
AVE = 3.674, MIN = 3.000, MAX = 4.045<CR><LF>
AVE = 4.001, MIN = 4.001, MAX = 4.001<CR><LF>

VOLTAVE<TM>
VOLTALL? 0 TO 2<TM>

This will return

2.034<CR><LF>
3.674<CR><LF>
4.001<CR><LF>

Command: VOLTALLH? (Voltage Query, All Channels, High Range)

Syntax: VOLTALL? [L],[CHANNEL STRING]<TM>
or VAH? [L],[CHANNEL STRING]<TM>

Mode: Analog or Digital

Purpose: Takes a voltage measurement within the ±50V range on all channels simultaneously.

Description: Parameter [L] is optional and defines whether labels should be included in the returned value. If [L] is specified, the returned values will be in one of the following two formats, depending on whether the VOLTFULL or VOLTAVE command is active. If VOLTFULL is active, the returned values will have the format:

AVE = <ave value>, MIN = <min value>, MAX = <max value><CR><LF>

If VOLTAVE is active, the returned values will have the format:

AVE = <ave value><CR><LF>

If [L] is omitted, the returned values will be in the format:
<ave value>, <min value>, <max value> (VOLTFULL active)
or <ave value> (VOLTAVE active)

[CHANNEL STRING] is a multicharacter string defining which channels are to have their voltage returned. [CHANNEL STRING] has the format:
[CHANNEL],[CHANNEL],...[CHANNEL]

where [CHANNEL] is:
a channel number between 0 and 31, or
a range of channels in the form:
<number 0 to 31> TO <number 0 to 31>

There may be any number of white spaces (including zero) before and after any TO.

This command checks only the ±50V range. If the voltage is outside this range, a VOLTAGE OVERFLOW or VOLTAGE UNDERFLOW message will be returned.

One voltage message will be returned for each channel specified in the [CHANNEL STRING], in the order given. The voltage measurement and syntax of the returned message is identical to that shown in the VOLT? command. A complete description of the voltage measurement is given in Appendix E.

Example: See the VOLTALL? command.

Command: VOLTALLL? (Voltage Query, All Channels, Low Range)

Syntax: VOLTALLL? [L],[CHANNEL STRING]<TM>
or VAL? [L],[CHANNEL STRING]<TM>

Mode: Analog or Digital

Purpose: Takes a voltage measurement within the ±10V range on all channels simultaneously.

Description: Parameter [L] is optional and defines whether labels should be included in the returned value. If [L] is specified, the returned values will be in one of the following two formats, depending on whether the VOLTFULL or VOLTAVE command is active. If VOLTFULL is active, the returned values will have the format:
AVE = <ave value>, MIN = <min value>, MAX = <max value><CR><LF>

If VOLTAVE is active, the returned values will have the format:

AVE = <ave value><CR><LF>

If [L] is omitted, the returned values will be in the format:
<ave value>, <min value>, <max value> or <ave value>.

[CHANNEL STRING] is a multicharacter string defining which channels are to have their voltage returned. [CHANNEL STRING] has the format:
[CHANNEL],[CHANNEL],...[CHANNEL]

where [CHANNEL] is:
a channel number between 0 and 31, or
a range of channels in the form:
<number 0 to 31> TO <number 0 to 31>

There may be any number of white spaces (including zero) before and after any TO.

This command checks only the ±10V range. If the voltage is outside this range, a VOLTAGE OVERFLOW or VOLTAGE UNDERFLOW message will be returned.

One voltage message will be returned for each channel specified in the [CHANNEL STRING], in the order given. The voltage measurement and syntax of the returned message is identical to that shown in the VOLT? command. A complete description of the voltage measurement is given in Appendix E.

Example: See the VOLTALL? command.

Command: VOLTAVE (Average Voltage)

Syntax: VOLTAVE<TM>
or VAV<TM>

Mode: Analog or Digital

Purpose: Specifies that only the average of the maximum and minimum voltages should be returned from one of the VOLT query commands.

Description: When this command is received, only the average of the maximum and minimum voltages will be returned from the VOLT?, VOLTH?, VOLTL?, VOLTALL?, VOLTALLH, or VOLTALLL? commands. See also the VOLTFULL command.

Example: VAV?<TM> The next time one of the VOLT query commands is issued, only the average of the maximum and minimum voltages will be returned.

Command: VOLTFULL (Complete Voltage)

Syntax: VOLTFULL<TM>
or VFL<TM>

Mode: Analog or Digital

Purpose: Specifies that the maximum, minimum, and average of the maximum and minimum voltages should be returned from one of the VOLT query commands.

Description: When this command is received, the maximum, minimum, and average of the maximum and minimum voltages will be returned from the VOLT?, VOLTH?, VOLTL?, VOLTALL?, VOLTALLH, or VOLTALLL? commands. This is the default on power-up. See also the VOLTAVE command.

Example: VFL?<TM> The next time one of the VOLT query commands is issued, the maximum, minimum, and average of the maximum and minimum voltages will be returned.

Command: VOLTH? (Voltage, High Range)

Syntax: VOLTH? [L],[B]<TM>
or VH? [L],[B]<TM>

Mode: Analog or Digital

Purpose: Returns the dc voltage of the specified input channel within the ±50V range.

Description: This command is identical to the VOLT? command, except that it will only take a measurement within the ±50V range. If the voltage is outside this range, a VOLTAGE OVERFLOW or VOLTAGE UNDERFLOW message will be returned.

Example: See the VOLT? command.

Command: VOLTL? (Voltage, Low Range)

Syntax: VOLTL? [L],[B]<TM>
or VL? [L],[B]<TM>

Mode: Analog or Digital

Purpose: Returns the dc voltage of the specified input channel within the ± 10V range.

Description: This command is identical to the VOLT? command, except that it will only take a measurement within the ± 10V range. If the voltage is outside this range, a VOLTAGE OVERFLOW or VOLTAGE UNDERFLOW message will be returned.

Example: See the VOLT? command.

Command: VOLTNEXT?

Syntax: VOLTNEXT?<TM>
or VN?<TM>

Mode: Analog or Digital

Purpose: Used to request another voltage message when reading the response of a VOLTALL? command.

Description: This command is included for use with controllers or software which require a command be given before each readback message. An example of a case where this might be needed is the VOLTALL? command, which may queue up multiple messages. This command is entirely optional.

Example:
VOLTALL? 4TO6<TM>
6.234, 6.234, 6.234<CR><LF>
VOLTNEXT?<TM>
7.110, 7.110, 7.110<CR><LF>
VOLTNEXT?<TM>
-2.222, -2.222, -2.222<CR><LF>

Optional use:

VOLTALL? 4TO6<TM>
VOLTNEXT?<TM>
6.234, 6.234, 6.234<CR><LF>
VOLTNEXT?<TM>
7.110, 7.110, 7.110<CR><LF>
VOLTNEXT?<TM>
-2.222, -2.222, -2.222<CR><LF>

Typical use of VOLTALL? without VOLTNEXT?:

VOLTALL? 4TO6<TM>
6.234, 6.234, 6.234<CR><LF>
7.110, 7.110, 7.110<CR><LF>
-2.222, -2.222, -2.222<CR><LF>

SYSFAIL, Self Test, and Initialization

The VX4286 Module will execute a self test at power-up, or upon direction of a VXIbus hard or soft reset condition, or upon command. The power-up self test consists of interface self test and an instrument self test. The commanded self test only executes the instrument self test. A VXIbus hard reset occurs when another device, such as the VXIbus Resource Manager, asserts the backplane line SYSRST*. A VXIbus soft reset occurs when another device, such as the VX4286's commander, sets the Reset bit in the VX4286's Control register.

During a power-up, or hard or soft reset, the following actions take place:

1) The SYSFAIL* (VME system-failure) line is set active, indicating that the module is executing an interface self test, and the Failed LED is lit. In the case of a soft reset, SYSFAIL* is set. However, all Tek/CDS commanders, such as the VX4521, will simultaneously set SYSFAIL INHIBIT. This is done to prevent the resource manager from prematurely reporting the failure of a card.

2) On completion of the interface self test, SYSFAIL* is de-asserted. If the test fails, the SYSFAIL* line remains active. If the interface self test passed, the SYSFAIL* line is released, and the module enters the VXIbus PASSED state (ready for normal operation). If it failed, the module enters the VXIbus FAILED state.

3) The instrument self test, as described in the IST command, is then executed. This tests the slave microprocessor, on-board field programmable gate arrays (FPGAs), on-board RAM, on-board non-volatile RAM, and all 32 inputs. If the self test fails, the module makes an internal record of what failure(s) occurred.

The default condition of the VX4286 Module after the completion of power-up self test is as follows:

General
Power LED: lit.
Mode: Analog mode.
Threshold level: 1.4V.
Range: ±10 volt range.
Trigger sense: Greater than threshold level (>).
Comparator status latches: cleared.
TTL Outputs: tri-stated.
Error buffer: cleared.
Error LED: off.
Readback type: error buffer.
Interrupts disabled.
Aperture time (for VOLT? command): 10 milliseconds.

Associated with Analog Mode
Module unarmed.
Inputs when in Analog mode: disabled.
EQU OUT signal polarity: active low.
Current time: zeroed.
Event buffer: cleared.
Analog readback format: returned by individual channel number, by event, relative time tag in seconds.

Channel names: CH<channel number> where <channel number> is a two digit number.
Analog display mode: real time.
Analog channel priority: 0 highest, 31 lowest.
Comparator status latches: cleared.
Flip bits: cleared (both sets).
Debounce counter time: 1/10 of a second.
Debounce enable: all channels disabled.
Source of Counter Synchronization Pulse: front panel P4.
Programmable hysteresis: off.

Associated with Digital Mode
Inputs when in Digital mode: enabled.
External Strobe: Disabled, strobe on readback of digital data.
Digital readback format: returned in ASCII hex, from digital input latches.
Digital display mode: real time.
Digital display byte order: 1,0, left to right.

Self test can also be run at any time during normal operation by using the IST command. At the end of a self test initiated by the IST command, the module is restored to its pre-test state (except that the digital input latches and analog comparator latches are cleared).

During a commanded self test SYSFAIL* is not asserted.

SYSFAIL* Operation

SYSFAIL* becomes active during power-up, hard or soft reset, self test, or if the module loses any of its power voltages. When the mainframe Resource Manager detects SYSFAIL* set, it will attempt to inhibit the line. This will cause the VX4286 Module to deactivate SYSFAIL* in all cases.

Command: VOLTNEXT?

Syntax: VOLTNEXT?<TM>
or VN?<TM>

Mode: Analog or Digital

Purpose: Used to request another voltage message when reading the response of a VOLTALL? command.

Description: This command is included for use with controllers or software which require a command be given before each readback message. An example of a case where this might be needed is the VOLTALL? command, which may queue up multiple messages. This command is entirely optional.

Example:

```
VOLTALL? 4TO6<TM>
 6.234, 6.234, 6.234<CR><LF>
VOLTNEXT?<TM>
 7.110, 7.110, 7.110<CR><LF>
VOLTNEXT?<TM>
 -2.222, -2.222, -2.222<CR><LF>
```

Optional use:

```
VOLTALL? 4TO6<TM>
VOLTNEXT?<TM>
 6.234, 6.234, 6.234<CR><LF>
VOLTNEXT?<TM>
 7.110, 7.110, 7.110<CR><LF>
VOLTNEXT?<TM>
 -2.222, -2.222, -2.222<CR><LF>
```

Typical use of VOLTALL? without VOLTNEXT?:

```
VOLTALL? 4TO6<TM>
 6.234, 6.234, 6.234<CR><LF>
 7.110, 7.110, 7.110<CR><LF>
 -2.222, -2.222, -2.222<CR><LF>
```

SYSFAIL, Self Test, and Initialization

The VX4286 Module will execute a self test at power-up, or upon direction of a VXIbus hard or soft reset condition, or upon command. The power-up self test consists of interface self test and an instrument self test. The commanded self test only executes the instrument self test. A VXIbus hard reset occurs when another device, such as the VXIbus Resource Manager, asserts the backplane line SYSRST*. A VXIbus soft reset occurs when another device, such as the VX4286's commander, sets the Reset bit in the VX4286's Control register.

During a power-up, or hard or soft reset, the following actions take place:

1) The SYSFAIL* (VME system-failure) line is set active, indicating that the module is executing an interface self test, and the Failed LED is lit. In the case of a soft reset, SYSFAIL* is set. However, all Tek/CDS commanders, such as the VX4521, will simultaneously set SYSFAIL INHIBIT. This is done to prevent the resource manager from prematurely reporting the failure of a card.

2) On completion of the interface self test, SYSFAIL* is de-asserted. If the test fails, the SYSFAIL* line remains active. If the interface self test passed, the SYSFAIL* line is released, and the module enters the VXIbus PASSED state (ready for normal operation). If it failed, the module enters the VXIbus FAILED state.

3) The instrument self test, as described in the IST command, is then executed. This tests the slave microprocessor, on-board field programmable gate arrays (FPGAs), on-board RAM, on-board non-volatile RAM, and all 32 inputs. If the self test fails, the module makes an internal record of what failure(s) occurred.

The default condition of the VX4286 Module after the completion of power-up self test is as follows:

General
Power LED: lit.
Mode: Analog mode.
Threshold level: 1.4V.
Range: ±10 volt range.
Trigger sense: Greater than threshold level (>).
Comparator status latches: cleared.
TTL Outputs: tri-stated.
Error buffer: cleared.
Error LED: off.
Readback type: error buffer.
Interrupts disabled.
Aperture time (for VOLT? command): 10 milliseconds.

Associated with Analog Mode
Module unarmed.
Inputs when in Analog mode: disabled.
EQU OUT signal polarity: active low.
Current time: zeroed.
Event buffer: cleared.

Event buffer: cleared.
Analog readback format: returned by individual channel number, by event, relative time tag in seconds.
Channel names: CH<channel number> where <channel number> is a two digit number.
Analog display mode: real time.
Analog channel priority: 0 highest, 31 lowest.
Comparator status latches: cleared.
Flip bits: cleared (both sets).
Debounce counter time: 1/10 of a second.
Debounce enable: all channels disabled.
Source of Counter Synchronization Pulse: front panel P4.
Programmable hysteresis: off.

Associated with Digital Mode
Inputs when in Digital mode: enabled.
External Strobe: Disabled, strobe on readback of digital data.
Digital readback format: returned in ASCII hex, from digital input latches.
Digital display mode: real time.
Digital display byte order: 1,0, left to right.

Self test can also be run at any time during normal operation by using the IST command. At the end of a self test initiated by the IST command, the module is restored to its pre-test state (except that the digital input latches and analog comparator latches are cleared).

During a commanded self test SYSFAIL* is not asserted.

SYSFAIL* Operation

SYSFAIL* becomes active during power-up, hard or soft reset, self test, or if the module loses any of its power voltages. When the mainframe Resource Manager detects SYSFAIL* set, it will attempt to inhibit the line. This will cause the VX4286 Module to deactivate SYSFAIL* in all cases.

Section 4
Programming Examples

This section contains example programs which demonstrate how the various programmable features of the VX4286 are used. The examples are written in BASIC using an IBM PC or equivalent computer as the system controller.

Definition of BASIC Commands

The programming examples in this manual are written in Microsoft GW BASIC, using the GW BASIC commands described below. If the programming language you are using does not conform exactly to these definitions, use the command in that language that will give the same result.

Command	Result
CALL ENTER (R$, LENGTH%, ADDRESS%, STATUS%)	The CALL ENTER statement inputs data into the string R$ from the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the input, the variable LENGTH% contains the number of bytes read from the instrument. The variable STATUS% contains the number '0' if the transfer was successful or an '8' if an operating system timeout occurred in the PC. Prior to using the CALL ENTER statement, the string R$ must be set to a string of spaces whose length is greater than or equal to the maximum number of bytes expected from the VX4286.
CALL SEND (ADDRESS%, WRT$, STATUS%)	The CALL SEND statement outputs the contents of the string variable WRT$ to the IEEE-488 instrument whose decimal primary address is contained in the variable ADDRESS%. Following the output of data, the variable STATUS% contains a '0' if the transfer was successful and an '8' if an operating timeout occurred in the PC.
END	Terminates the program.
FOR/NEXT	Repeats the instructions between the FOR and NEXT statements for a defined number of iterations.
GOSUB n	Runs the subroutine beginning with line n. EX: GOSUB 750 - runs the subroutine beginning on line 750. The end of the subroutine is delineated with a RETURN statement. When the subroutine reaches the RETURN statement, execution will resume on the line following the GOSUB command.
GOTO n	Program branches to line n. EX: GOTO 320 - directs execution to continue at line 320.

IF/THEN	Sets up a conditional IF/THEN statement. Used with other commands, such as PRINT or GOTO, so that IF the stated condition is met, THEN the command following is effective. EX: IF I = 3 THEN GOTO 450 - will continue operation at line 450 when the value of variable I is 3.
REM	All characters following the REM command are not executed. REM statements are used for documentation and user instructions. EX: REM **CLOSE ISOLATION RELAYS**
RETURN	Ends a subroutine and returns operation to the line after the last executed GOSUB command.
<CR>	Carriage Return character, decimal 13.
<LF>	Line Feed character, decimal 10.

Programming Example In BASIC

The following sample BASIC program shows how commands for the VX4286 might be used. This example assumes that the VX4286 has logical address 24 and is installed in a VXIbus mainframe that is controlled through an IEEE-488 interface from an external system controller, such as an IBM PC or equivalent using a Capital Equipment Corp. IEEE-488 interface. The VXIbus IEEE-488 interface is assumed to have an IEEE-488 primary address of decimal 21 and to have converted the VX4286 Module's logical address to an IEEE-488 primary address of decimal 24.

Following each example, the data sent to and returned from the module is shown, with data returned by the module shown underlined.

Example:

```
010 GOSUB 9000              ' LOCATE CEC CARD
100 DEF SEG = CECLOC        ' DEFINES MEMORY LOCATION FOR I/O CARD
200 '
201 ' INITIALIZE CEC CALLS
202 '
210 INIT = 0:               ' CALL INIT (GPIB%,LEVEL%)
220 SEND = 9:               ' CALL SEND (PCX%, WRT$, STATUS%)
230 SPOLL = 12:             ' CALL SPOLL (PCX%, POLL%, STATUS%)
240 ENTER = 21:             ' CALL ENTER (RD$, LENGTH%, PCX%, STATUS%)
300 '
301 ' DEFINE ADDRESS
302 '
310 GPIB% = 0:              ' DEFINES SLOT 0 ADDRESS
310                         ' TEK/CDS SLOT 0 CARDS ARE TYPICALLY PROGRAMMED
320                         ' TO ADDRESS 0 OR 1
320 CADD% = 25: PADD% = CADD%
330                         ' DEFINES VX4286 ADDRESS
```

```
330 LEVEL% = 0:              ' DEFINES GPIB% AS A BUS CONTROLLER
340 '
351 ' INITIALIZE CEC CARD, MEMORY AND DISPLAY
362 '
370 CALL INIT(GPIB%, LEVEL%): IF STATUS% < > 0 THEN BEEP: STOP
380 RD$ = SPACE$(80)         ' DEFINE SPACE FOR READBACK
390 CLS
500 '*******************
501 ' USE ANALOG MODE OF VX4286, CONTINUALLY PRINT ALL CHANNELS
502 ' ON WRONG SIDE OF THRESHOLD
503 '*******************
504 PRINT "ANALOG MODE"
510 WRT$ = "RST;TRG 0>4.00;TRG 1TO6<3.00;ARM ON;EQU 0TO31;ERR?"
520 GOSUB 5000               ' WRITE TO VX4286
530 GOSUB 6000               ' READ VX4286
540 PRINT RD$                ' PRINT ANY POSSIBLE ERRORS
600 WRT$ = "DATA? R":GOSUB 5000
610                          ' READ BACK COLLECTED INFORMATION
620 GOSUB 6000
650 PRINT RD$                ' PRINT AN ENTRY IN THE BUFFER
1500 '*******************
1501 ' USE ANALOG MODE OF VX4286, FLIP TRIGGER SENSE CONTINUALLY
1503 '*******************
1504 PRINT "ANALOG MODE (FLIP ENABLED)"
1510 WRT$ = "RST;TRG 0>4.00;TRG 1TO6<3.00;ARM ON;FLIPCONT;EQU 0TO31;ERR?"
1520 GOSUB 5000              ' WRITE TO VX4286
1530 GOSUB 6000              ' READ VX4286
1540 PRINT RD$               ' PRINT ANY POSSIBLE ERRORS
1600 WRT$ = "DATA?":GOSUB 5000
1610                         ' READ BACK COLLECTED INFORMATION
1620 GOSUB 6000
1650 PRINT RD$               ' PRINT AN ENTRY IN THE BUFFER
2500 '*******************
2501 ' USE DIGITAL MODE OF VX4286
2502 ' READ RESULTS
2503 '*******************
2504 PRINT "DIGITAL MODE"
2510 WRT$ = "DIGITAL;TRG 0TO31>3.00;FMTDIG BINA;ENB 0TO31;STB S";GOSUB 5000
2520 WRT$ = "DATA?";GOSUB 5000
2530 FOR I = 0 UNTIL 10
2530    GOSUB 6000
2540    PRINT RD$
2550 NEXT I
2560 STOP
5000 ' WRITE SUBROUTINE
5010 WRT$ = WRT$ + CHR$(10)
5020 CALL SEND(CADD%,WRT$,STATUS%)
5030 RETURN
6000 ' READ SUBROUTINE
6010 CALL ENTER(RD$, LENGTH%, CADD%, STATUS%)
6020 RETURN
9000 ' LOCATE CEC BOARD
9010 FOR I = &H40 TO &HEC STEP &H4
```

```
9020 FAILED = 0: DEF SEG = (I * &H100)
9030 IF CHR$(PEEK(50)) < > "C" THEN FAILED = 1
9040 IF CHR$(PEEK(51)) < > "E" THEN FAILED = 1
9050 IF CHR$(PEEK(52)) < > "C" THEN FAILED = 1
9060 IF FAILED = 0 THEN CECLOC = (I * &H100): I = &HEC
9070 NEXT I
9080 RETURN
9999 END
```

Appendix A
VXIbus Operation

The VX4286 Module is a C size single slot VXIbus Message Based Word Serial instrument. It uses the A16, D16 VME interface available on the backplane P1 connector and does not require any A24 or A32 address space. The module is a D16 interrupter.

The VX4286 is neither a VXIbus commander nor a VMEbus master, and therefore it does not have a VXIbus Signal register. The VX4286 is a VXIbus message based servant.

The module supports both the Normal Transfer Mode and the Fast Handshake Mode of the VXIbus, using the Write Ready and Read Ready bits of the module's Response register.

A Normal Transfer Mode Read of the VX4286 proceeds as follows:

1. The commander reads the VX4286's Response register and checks if the Write Ready and DOR bits are true. IF they are, the commander proceeds to the next step. If not, the commander continues to poll these bits until they become true.

2. The commander writes the Byte Request command (0DEFFh) to the VX4286's Data Low register.

3. The commander reads the VX4286's Response register and checks if the Read Ready and DOR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll these bits until they become true.

4. The commander reads the VX4286's Data Low register.

A Normal Transfer Mode Write to the VX4286 Module proceeds as follows:

1. The commander reads the VX4286's Response register and checks if the Write Ready and DIR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll the Write Ready and DIR bits until they are true.

2. The commander writes the Byte Available command which contains the data (0BCXX or 0BDXX, depending on the End bit) to the VX4286's Data Low register.

The VX4286 Module also supports the Fast Handshake mode during readback. In this mode, the module is capable of transferring data at optimal backplane speed without the need of the commander's testing any of the handshake bits. The VX4286 Module asserts BERR* to switch from Fast Handshake Mode to Normal Transfer Mode, per VXI Specification. The VX4286's Read Ready, Write Ready, DIR and DOR bits react properly, in case the commander does not support the Fast Handshake Mode.

A Fast Handshake Transfer Mode Read of the VX4286 proceeds as follows:

1. The commander writes the Byte Request command (0DEFFh) to the VX4286's Data Low register.

2. The commander reads the VX4286's Data Low register.

The VX4286 Module has no registers beyond those defined for VXIbus message based devices. All communications with the module are through the Data Low register, the Response register, or the VXIbus interrupt cycle. Any attempt by another module to read or write to any undefined location of the VX4286's address space may cause incorrect operation of the module.

CAUTION

If the user's mainframe has other manufacturer's computer boards operating in the role of VXIbus foreign devices, the assertion of BERR (as defined by the VXIbus Specification) may cause operating problems on these boards.*

As with all VXIbus devices, the VX4286 has registers located within a 64 byte block in the A16 address space.

The base address of the VX4286 device's registers is determined by the device's unique logical address and can be calculated as follows:

Base Address = V * 40H + C000H

where V is the device's logical address as set by the Logical Address switches.

VX4286 Configuration Registers

Below is a list of the VX4286 Configuration registers with a complete description of each. In this list, RO = Read Only, WO = Write Only, R = Read, and W = Write. The offset is relative to the module's base address.

REGISTER DEFINITIONS

Register	Address	Type	Value (Bits 15-0)
ID Register	0000H	RO	1011 1111 1111 1100 (BFFCh)
Device Type	0002H	RO	See Device Type definition below
Status	0004H	R	Defined by the state of the interface
Control	0004H	W	0111 1111 1111 110X (7FFCh or 7FFDh)
Offset	0006H	WO	Not used
Protocol	0008H	RO	1111 0111 1111 1111 (F7FFh)
Response	000AH	RO	Defined by state of the interface
Data High	000CH		Not used
Data Low	000EH	W	See Data Low definition below
Data Low	000EH	R	See Data Low definition below

REGISTER BIT DEFINITIONS

ID: BFFCh

Device: F6E1h

Protocol: F7FFh

Word Serial Commands

A write to the Data Low register causes this module to execute some action based on the data written. This section describes the device-specific Word Serial commands this module responds to and the results of these commands.

Read Protocol command response: FE6Bh

Appendix B
Input/Output Connections

P4

1	Input 0
2	Input 1
3	Input 2
4	Input 3
5	Input 4
6	Input 5
7	Input 6
8	Input 7
9	Input 8
10	Input 9
11	Input 10
12	Input 11
13	Input 12
14	Input 13
15	Input 14
16	Input 15
17	Counter Synchronization Signal (input)
18-33	GND
34	TTL Output 0
35	TTL Output 1
36	TTL Output 2
37	TTL Output 3
38	TTL Output 4
39	TTL Output 5
40	TTL Output 6
41	TTL Output 7
42	GND
43	TTL Output 8
44	TTL Output 9
45	TTL Output 10
46	TTL Output 11
47	TTL Output 12
48	TTL Output 13
49	TTL Output 14
50	TTL Output 15

P5

1	Input 16
2	Input 17
3	Input 18
4	Input 19
5	Input 20
6	Input 21
7	Input 22
8	Input 23
9	Input 24
10	Input 25
11	Input 26
12	Input 27
13	Input 28
14	Input 29
15	Input 30
16	Input 31
17	Daughter Board Common (input)
18-33	GND
34	TTL Output 16
35	TTL Output 17
36	TTL Output 18
37	TTL Output 19
38	TTL Output 20
39	TTL Output 21
40	TTL Output 22
41	TTL Output 23
42	GND
43	TTL Output 24
44	TTL Output 25
45	TTL Output 26
46	TTL Output 27
47	TTL Output 28
48	TTL Output 29
49	TTL Output 30
50	TTL Output 31

STB/ARM BNC	Strobe/Arm signal (input)
EQU OUT BNC	EQU Output signal (output)

Appendix C
VXI Glossary

The terms in this glossary are defined as used in the VXIbus System. Although some of these terms may have different meanings in other systems, it is important to use these definitions in VXIbus applications. Terms which apply only to a particular instrument module are noted.

Term	Definition
Accessed Indicator	An amber LED indicator that lights when the module identity is selected by the Resource Manager module, and flashes during any I/O operation for the module.
ACFAIL*	A VMEbus backplane line that is asserted under these conditions: 1) by the mainframe Power Supply when a power failure has occurred (either ac line source or power supply malfunction), or 2) by the front panel ON/STANDBY switch when switched to STANDBY.
A-Size Card	A VXIbus instrument module that is 100.0 by 160 mm by 20.32 mm (3.9 by 6.3 in by 0.8 in), the same size as a VMEbus single-height short module.
Asynchronous Communication	Communications that occur outside the normal "command-response" cycle. Such communications have higher priority than synchronous communication.
Backplane	The printed circuit board that is mounted in a VXIbus mainframe to provide the interface between VXIbus modules and between those modules and the external system.
B-Size Card	A VXIbus instrument module that is 233.4 by 160 mm by 20.32 mm (9.2 by 6.3 in by 0.8 in), the same size as a VMEbus double-height short module.
Bus Arbitration	In the VMEbus interface, a system for resolving contention for service among VMEbus Master devices on the VMEbus.
Bus Timer	A functional module that measures the duration of each data transfer on the Data Transfer Bus (DTB) and terminates the DTB cycle if the duration is excessive. Without the termination capability of this module, a Bus Master attempt to transfer data to or from a non-existent Slave location could result in an infinitely long wait for the Slave response.
Client	In shared memory protocol (SMP), that half of an SMP channel that does not control the shared memory buffers.

CLK10 A 10-MHz, ±100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1-12 on P2. It is distributed to each module slot as a single source, single destination signal with a matched delay of under 8 ns.

CLK100 A 100-MHz, ±100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1-12 on P3. It is distributed to each module slot in synchronous with CLK10 as a single source, single destination signal with a maximum system timing skew of 2 ns, and a maximum total delay of 8 ns.

Commander In the VXIbus interface, a device that controls another device (a servant). A commander may be a servant of another commander.

Command A directive to a device. There are three types of commands:

In Word Serial Protocol, a 16-bit imperative to a servant from its commander.

In Shared Memory Protocol, a 16-bit imperative from a client to a server, or vice versa.

In a Message, an ASCII-coded, multi-byte directive to any receiving device.

Communication Registers In word serial protocol, a set of device registers that are accessible to the commander of the device. Such registers are used for inter-device communications, and are required on all VXIbus message-based devices.

Configuration Registers A set of registers that allow the system to identify a (module) device type, model, manufacturer, address space, and memory requirements. In order to support automatic system and memory configuration, the VXIbus standard specifies that all VXIbus devices have a set of such registers, all accessible from P1 on the VMEbus.

C-Size Card A VXIbus instrument module that is 340.0 by 233.4 mm by 30.48 mm (13.4 by 9.2 in by 1.2 in).

Custom Device A special-purpose VXIbus device that has configuration registers so as to be identified by the system and to allow for definition of future device types to support further levels of compatibility.

Data Transfer Bus One of four buses on the VMEbus backplane. The Data Transfer Bus allows Bus Masters to direct the transfer of binary data between Masters and Slaves.

DC SUPPLIES Indicator A red LED indicator that illuminates when a DC power fault is detected on the backplane.

Device Specific

Protocol A protocol for communication with a device that is not defined in the VXIbus specification.

D-Size Card A VXIbus instrument module that is 340.0 by 366.7 mm by 30.48 mm (13.4 x 14.4 in x 1.2 in).

DTB See Data Transfer Bus.

DTB Arbiter A functional module that accepts bus requests from Requester modules and grants control of the DTB to one Requester at a time.

DUT Device Under Test.

ECLTRG Six single-ended ECL trigger lines (two on P2 and four on P3) that function as inter-module timing resources, and that are bussed across the VXIbus subsystem backplane. Any module, including the Slot 0 module, may drive and receive information from these lines. These lines have an impedance of 50 ohms; the asserted state is logical High.

Embedded Address An address in a communications protocol in which the destination of the message is included in the message.

ESTST Extended STart/STop protocol; used to synchronize VXIbus modules.

Extended Self Test Any self test or diagnostic power-up routine that executes after the initial kernel self test program.

External System Controller The host computer or other external controller that exerts overall control over VXIbus operations.

FAILED Indicator A red LED indicator that lights when a device on the VXIbus has detected an internal fault. This might result in the assertion of the SYSFAIL* line.

IACK Daisy Chain Driver The circuit that drives the VMEbus Interrupt Acknowledge daisy chain line that runs continuously through all installed modules or through jumpers across the backplane.

ID-ROM An NVRAM storage area that provides for non-volatile storage of diagnostic data.

Instrument Module A plug-in printed circuit board, with associated components and shields, that may be installed in a VXIbus mainframe. An instrument module may contain more than one device. Also, one device may require more than one instrument module.

Interface Device A VXIbus device that provides one or more interfaces to external equipment.

Interrupt Handler — A functional module that detects interrupt requests generated by Interrupters and responds to those requests by requesting status and identity information.

Interrupter — A device capable of asserting VMEbus interrupts and performing the interrupt acknowledge sequence.

IRQ — The Interrupt ReQuest signal, which is the VMEbus interrupt line that is asserted by an Interrupter to signify to the controller that a device on the bus requires service by the controller.

Local Bus — A daisy-chained bus that connects adjacent VXIbus slots.

Local Controller — The instrument module that performs system control and external interface functions for the instrument modules in a VXIbus mainframe or several mainframes. See Resource Manager.

Local Processor — The processor on an instrument module.

Logical Address — The smallest functional unit recognized by a VXIbus system. It is often used to identify a particular module.

Mainframe

Card Cage — For example, the Tektronix VX1400 Mainframe, an operable housing that includes 13 C-size VXIbus instrument module slots.

Memory Device — A storage element (such as bubble memory, RAM, and ROM) that has configuration registers and memory attributes (such as type and access time).

Message — A series of data bytes that are treated as a single communication, with a well defined terminator and message body.

Message Based Device — A VXIbus device that supports VXI configuration and communication registers. Such devices support the word serial protocol, and possibly other message-based protocols.

MODID Lines — Module/system identity lines.

Physical Address — The address assigned to a backplane slot during an access.

Power Monitor — A device that monitors backplane power and reports fault conditions.

P1 — The top-most backplane connector for a given module slot in a vertical mainframe such as the Tektronix VX1400. The left-most backplane connector for a given slot in a horizontal mainframe.

P2 — The bottom backplane connector for a given module slot in a vertical C-size mainframe such as the VX1400; or the middle backplane

	connector for a given module slot in a vertical D-size mainframe such as the VX1500.
P3	The bottom backplane connector for a given module slot in a vertical D-size mainframe such as the Tektronix VX1500.
Query	A form of command that allows for inquiry to obtain status or data.
READY Indicator	A green LED indicator that lights when the power-up diagnostic routines have been completed successfully. An internal failure or failure of +5-volt power will extinguish this indicator.
Register Based Device	A VXIbus device that supports VXI register maps, but not high level VXIbus communication protocols; includes devices that are register-based servant elements.
Requester	A functional module that resides on the same module as a Master or Interrupt Handler and requests use of the DTB whenever its Master or Interrupt Handler requires it.
Resource Manager	A VXIbus device that provides configuration management services such as address map configuration, determining system hierarchy, allocating shared system resources, performing system self test diagnostics, and initializing system commanders.
Self Calibration	A routine that verifies the basic calibration of the instrument module circuits, and adjusts this calibration to compensate for short- and long-term variables.
Self Test	A set of routines that determine if the instrument module circuits will perform according to a given set of standards. A self test routine is performed upon power-up.
Servant	A VXIbus message-based device that is controlled by a commander.
Server	A shared memory device that controls the shared memory buffers used in a given Shared Memory Protocol channel.
Shared Memory Protocol	A communications protocol that uses a block of memory that is accessible to both client and server. The memory block operates as a message buffer for communications.
Slot 0 Controller	See Slot 0 Module. Also see Resource Manager.
Slot 0 Module	A VXIbus device that provides the minimum VXIbus slot 0 services to slots 1 through 12 (CLK10 and the module identity lines), but that may provide other services such as CLK100, SYNC100, STARBUS, and trigger control.
SMP	See Shared Memory Protocol.
STARX	Two (2) bi-directional, 50 ohm, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and

matched delay lines connect slot 0 and each of slots 1 through 12 in a mainframe. The delay between slots is less than 5 nanoseconds, and the lines are well matched for timing skew.

STARY Two (2) bi-directional, 50 ohm, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a mainframe. The delay between slots is less than 5 nanoseconds, and the lines are well matched for timing skew.

STST STart/STop protocol; used to synchronize modules.

SYNC100 A Slot 0 signal that is used to synchronize multiple devices with respect to a given rising edge of CLK100. These signals are individually buffered and matched to less than 2ns of skew.

Synchronous Communications A communications system that follows the "command-response" cycle model. In this model, a device issues a command to another device; the second device executes the command; then returns a response. Synchronous commands are executed in the order received.

SYSFAIL* A signal line on the VMEbus that is used to indicate a failure by a device. The device that fails asserts this line.

System Clock Driver A functional module that provides a 16-MHz timing signal on the Utility Bus.

System Hierarchy The tree structure of the commander/servant relationships of all devices in the system at a given time. In the VXIbus structure, each servant has a commander. A commander may also have a commander.

Test Monitor An executive routine that is responsible for executing the self tests, storing any errors in the ID-ROM, and reporting such errors to the Resource Manager.

Test Program A program, executed on the system controller, that controls the execution of tests within the test system.

Test System A collection of hardware and software modules that operate in concert to test a target DUT.

TTLTRG Open collector TTL lines used for inter-module timing and communication.

VXIbus Subsystem One mainframe with modules installed. The installed modules include one module that performs slot 0 functions and a given complement of instrument modules. The subsystem may also include a Resource Manager.

Word Serial

Protocol	A VXIbus word oriented, bi-directional, serial protocol for communications between message-based devices (that is, devices that include communication registers in addition to configuration registers).
Word Serial Communications	Inter-device communications using the Word Serial Protocol.
WSP	See Word Serial Protocol.
10-MHz Clock	A 10 MHz, ± 100 ppm timing reference. Also see CLK10.
100-MHz Clock	A 100 MHz, ± 100 ppm clock synchronized with CLK10. Also see CLK100.
488-To-VXIbus Interface	A message based device that provides for communication between the IEEE-488 bus and VXIbus instrument modules.

Appendix D
Resetting Equation Period

The equation period is the time period bounded by the time when the defined Boolean equation (EQU command) first becomes active, and the time when it becomes true. At this time, the EQU OUT signal pulses, and an interrupt occurs (if enabled).

When the module is first reset or powered up, the equation period starts when the module both becomes armed (ARM command) and an equation has been defined (EQU command). Once the equation period has begun, when the equation has been satisfied, the EQU OUT signal pulses. From this point on, any transition to the "wrong" side of the threshold on an enabled channel will cause the EQU OUT signal to pulse until the equation period is reset.

If the equation period is to be reset, however, care must be taken in command ordering so that the period is reset at the desired time. The problem is illustrated in the following example:

Assume EQU 4 + 5 previously sent:
1) REENB 4,5
2) Assume channel 5 now transitions before the EQURST command can be sent
3) EQURST
4) Assume channel 4 now transitions (EQU OUT signal will not occur here)

Note that in this example, EQU OUT signal does not pulse during step 4, as might be expected. This is because channel 5 disabled itself in step 2 (assuming its Flip Continuous bit was not set). The EQU OUT signal will occur the next time channel 5 is re-enabled with a EQU,REENB or DATA? R command. To prevent this problem, the EQURST command is integrated into the REENB and DATA? commands as option [Q]. Following are some examples of different methods of resetting the equation period.

Example 1: Resetting period upon data readback (Q option of DATA? command)

Assume EQU 4 + 5 previously sent:
1) DATA? Q or DATA? R,Q until all data read back
2) Assume channel 5 now transitions
3) Assume channel 4 now transitions (EQU OUT signal occurs here)

In the above example, the equation period restarts when the last entry was read from the Event buffer with the DATA? Q or DATA? R,Q command in step 1.

Example 2: Resetting period upon forcing all channels to be re-enabled (Q option of REENB in conjunction with F option)

Assume EQU 4 + 5 previously sent:

1) REENB Q,F,4,5 or EQU F,4 + 5
2) Any events that occur before this REENB or EQU command are immaterial with respect to the equation period.
3) Assume channel 4 now transitions
4) Assume channel 5 now transitions (EQU OUT signal occurs here)

In the above example, the equation period begins in step 1, as all channels are forcibly enabled (F option). This example, however, may lead to multiple entries in the Event buffer.

Example 3: Resetting period by clearing Event buffer (Q option of REENB command in conjunction with E option)

Assume EQU 4 + 5 previously sent:
1) REENB Q,E,4,5 or EQU E,4 + 5
2) Any events that occur before this REENB or EQU command are immaterial with respect to the equation.
3) Assume channel 4 now transitions
4) Assume channel 5 now transitions (EQU OUT signal occurs here)

In the above example, the equation period begins in step 1, as all channels are enabled. The Event buffer is cleared on this command (E option).

Example 4: Resetting period by disarming module.

Assume EQU 4 + 5 previously sent:
1) ARM OFF
2) D? until all entries read back (or RST EVNT)
3) REENB Q,4,5 or EQU 4 + 5
4) ARM ON
5) Any events that occur before the ARM ON command are immaterial with respect to the equation.
6) Assume channel 4 now transitions
7) Assume channel 5 now transitions (EQU OUT signal occurs here)

In this example, the equation period begins in step 4, when the module is rearmed.

Appendix E
Voltage Measurement on the VX4286

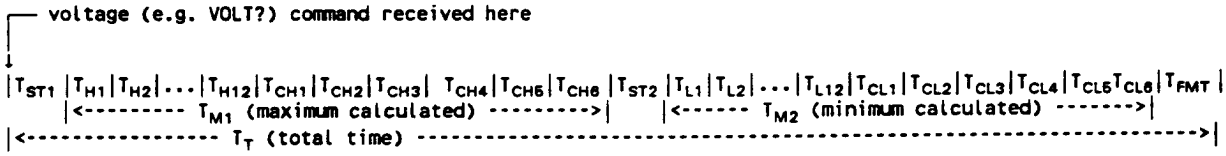
For full accuracy, the input signal must be a repeatable waveform (a DC signal can be seen as repeatable at a repetition period of 0), and the repetition period must be less than the programmed aperture time. This module will return the result of a nonrepeatable, random signal (or where the repetition period is greater than the aperture time) as the DC voltage of the waveform at some particular point of time during the measurement interval.

The execution time of a voltage measurement depends on:

- the aperture time,
- which voltage command has been sent,
- whether VOLTAVE or VOLTFULL command has been sent, and
- whether of not the 15 millivolts of voltage hysteresis on each input is being compensated for.

A table of execution times is given at the end of this Appendix.

The effect of these factors can be seen in the following diagram, which shows the sequence of events during the voltage measurement.



T_{M1}: measurement interval (maximum voltage)
T_{M2}: measurement interval (minimum voltage)
T_T: total time for voltage command

T_{ST1} + T_{ST2}: Setup time

T_{H1}: most significant bit determined (maximum voltage)
T_{H2}: 2nd most significant bit determined (maximum voltage)
...
T_{H12}: least significant bit determined (maximum voltage)

T_{CH1} - T_{CH6}: voltage hysteresis is compensated for (maximum voltage)

T_{L1}: most significant bit determined (minimum voltage)
T_{L2}: 2nd most significant bit determined (minimum voltage)
...
T_{L12}: least significant bit determined (minimum voltage)

T_{CL1} - T_{CL6}: voltage hysteresis is compensated for (minimum voltage)

T_{Fmt}: result formatted (VOLT?, VOLTL?, VOLTH? commands)

The time periods of T_{Hx}, T_{CHx}, T_{Lx}, and T_{CLx} are equivalent to aperture time, as specified by the APER command, and are all the same (default 10 msec).

When the command is received, a setup procedure takes place (T_{ST1}). Then the twelve bits of voltage are determined (T_{H1} to T_{H12}), and then the 15 millivolts of voltage hysteresis is compensated for (T_{CH1} to T_{CH6}). Voltage hysteresis compensation takes anywhere from two to six aperture times (in other words, T_{CH3} through T_{CH6} are not always executed). At this point, the maximum value has been calculated. This sequence is then repeated (T_{ST2}, T_{L1} to T_{H12}, T_{CL1} to T_{CL6}) to determine the minimum voltage. If the command was VOLT?, VOLTL?, or VOLTH?, the result is formatted at this point (T_{FMT}). If the command was VOLTALL?, VOLTALLL?, or VOLTALLH?, the result of each channel is formatted each time this module is read back for its result.

Successive Approximation Method

The successive approximation method of voltage measurement is used. It begins by assuming the input signal is at a voltage of half the range. For the ±10V range, this is 0V.

Then for twelve steps, it determines first whether to add or subtract 5 volts (half the most significant bit), then whether to add or subtract 2.5 volts, then 1.25 volts and so forth, each time decreasing the add/subtract value by a factor of 2 until it is down to 20/(2^12) which represents the least significant bit of the voltage measurement.

The determination of whether to add or subtract each time is obtained during the periods T_{H1}, T_{H2}, ... T_{H12}. For the first period T_{H1}, the module is set up so that if the input signal goes above 0 volts at ANY time within this period, a latch is set. At the end of this period, if the latch is set, 5 volts is added to 0 volts. If not, 5 volts is subtracted. For the next period, the latch is cleared, and then the module is set up so that if the input signal goes above the newly calculated voltage (5 or -5 volts) during time T_{H2}, the latch is set. The value of 2.5 volts is added if the latch was set, subtracted otherwise. This continues, with new voltages being calculated, through period T_{H12}, at which time the calculated voltage represents the maximum voltage of the input waveform.

During times T_{CH1} through T_{CH6}, the module compensates for the onboard hysteresis (15 mV), but only if it is operating in the ±10V range. The compensation sequence does not take place for the ±50V range. For faster voltage measurement, the compensation stage can be omitted (VHYST command), at a small loss in accuracy (7 mV).

For the minimum voltage, the module then repeats the identical process (T_{ST2}, T_{L1} to T_{L12}, T_{CL1} to T_{CL4}), but this time checks to see if the input voltage goes BELOW the calculated voltage.

If the VOLT? or VOLTALL? commands are being used (auto ranging), the sequence T_{ST1} to T_{CL4} will be repeated twice if the voltage is determined not to be within ±10 volts.

As mentioned at the beginning of this section, the signal should be a repeatable signal (or DC signal), repeatable within an aperture time. If this is not the case, a voltage that was present somewhere within the measurement interval T_{M1} or T_{M2} will be returned.

Execution Times

The total execution time for the voltage commands are listed in the following tables. The first table gives the times for default conditions and fastest conditions. The default conditions are: aperture = 10 msecs; VHYST = ON; VOLTFULL. The fastest conditions are: aperture = 0.1 msec; VHYST = OFF; VOLTAVE.

	DEFAULT CONDITIONS		FASTEST CONDITIONS	
	Single Channel	32 Channels	Single Channel	32 Channels
VOLTL?,VOLT?[1]	420	N/A	36.4	N/A
VOLTH?	290	N/A	36.4	N/A
VOLT?[2]	780	N/A	50.8	N/A
VOLTALLL?,VOLTALL?[3]	510	850	98	220
VOLTALLH?	340	680	96	220
VOLTALL?[4]	940	1280	170	300

1 applied voltage is between ± 10 volts
2 applied voltage is greater than + 10 volts or less than -10 volts
3 applied voltages of all 32 input channels are between + /- 10 volts
4 applied voltage of any one of the 32 input channels is greater than + 10 volts or less than -10 volts

All times are in milliseconds.

The second table gives equations to calculate the execution time in the more general case. Note that the controller may add some of its own time to these numbers.

	VHYST OFF VOLTFULL	VHYST OFF VOLTAVE	VHYST ON VOLTFULL	VHYST ON VOLTAVE
VOLTL?,VOLT?[1]	43 + (24*A)	34 + (24*A)	54 + (36*A)	47 + (36*A)
VOLTH?	43 + (24*A)	34 + (24*A)	41 + (24*A)	34 + (24*A)
VOLT?[2]	53 + (48*A)	46 + (48*A)	59 + (72*A)	52 + (72*A)
VOLTALLL?,VOLTALL?[3]	90 + (24*A) + (11*N)	90 + (24*A) + (4*N)	138 + (36*A) + (11*N)	138 + (36*A) + (4*N)
VOLTALLH?	90 + (24*A) + (11*N)	90 + (24*A) + (4*N)	89 + (24*A) + (11*N)	89 + (24*A) + (4*N)
VOLTALL?[4]	162 + (48*A) + (11*N)	162 + (48*A) + (4*N)	205 + (72*A) + (11*N)	205 + (72*A) + (4*N)

1 applied voltage is between ± 10 volts
2 applied voltage is greater than + 10 volts or less than -10 volts
3 applied voltages of all 32 input channels are between + /- 10 volts
4 applied voltage of any one of the 32 input channels is greater than + 10 volts or less than -10 volts

All times are in milliseconds.

A is the aperture time. N is the number of channels specified. For VOLTALLL?, VOLTALLH?, and VOLTALL? commands, formatting of the data into ASCII characters takes place when the card is read back. For instance, the time of the VOLTALLL? command is 138 + (36*A) + (11*N). The VOLTALL? command in this case will take 90 + (36*A) msecs to execute. Each readback of the voltage thereafter will take 11 msecs per readback.

For VOLTL?, VOLTH?, VOLT? commands, formatting of the data into ASCII characters takes place when the command is received (T_{FMT}). The time for the VOLTL? command is 54 + (36*A). Here the 54 represents the setup (T_{ST1} + T_{ST2}) and formatting (T_{FMT}) time.

Appendix A: Performance Verification

This Performance Verification procedure contains test sequences suitable for determining if the VX4286 functions, was adjusted properly, and meets the performance characteristics as warranted.

The following skills are required to perform this procedure:

- Thorough knowledge of test instrument operation and proper measurement techniques
- Knowledge of VXIbus system components and command language programming
- Ability and facility to construct interconnections and fixtures as needed to perform the procedure

General Information and Conventions

The following conventions apply throughout this procedure:

- Each test sequence begins with a table, similar to the one below, which provides information and requirements specific to that section. The item number appearing after each piece of equipment refers to an entry in Table A–1, *Required Test Equipment.* Immediately following the table, you will be given instructions for interconnecting the VX4286 under-test and for checking the performance parameters. Results may then be recorded on a photocopy of the Test Record which may be found on page A–26.

Equipment Requirements	Digital Oscilloscope (item 1) Coaxial Cable, two (item 6) DD50S Interconnect Adapter (item 5)
Prerequisites	All prerequisites listed on page A–22

- This procedure assumes that you will be using a VX4521 Slot 0 Resource Manager and a National Instruments PC-GPIB controller configuration as described in Table A–3. You will be instructed to use the corresponding National Interface Bus Interactive Control (ibic) commands to set up the VX4286 under-test and other associated VXIbus test instruments. Please refer to the NI-488.2M User Manual for additional information. If you are using a different controller and software, simply substitute the appropriate commands to achieve equivalent result.

- VX4286 commands may be sent in upper or lower case. To avoid confusion between alphanumeric characters, for example between a one (1) and an “L” or a zero (0) and and the letter “o”, all commands are illustrated in the case which provides the greatest visual distinction. Although you may use any combination of upper and/or lower case to enter a command sequence, use care when reading and interpreting these characters in this procedure.

Prerequisites

The test sequences in this procedure are valid under the following conditions:

- The VX4286 module covers are in place and the module is installed in an approved VXIbus mainframe as described in Section 2 of the User Manual
- The VX4286 has passed the power-on self test
- The VX4286 has been operating for a warm-up period of 10 minutes in an ambient environment as specified in Section 1 of the User Manual

Equipment Required

This procedure uses traceable test equipment as specified in Table A–1 to directly check warranted characteristics. You may use instrumentation other than the recommended example if it meets the minimum requirements.

Table A–1: Required Test Equipment

Item Number and Description	Minimum Requirements	Example	Purpose
1. Digital Oscilloscope with probes (two)	300 MHz bandwidth; 1.5% DC vertical accuracy	Tektronix TDS 460	Checking signal timing, amplitude, and phase
2. Function Generator	Frequency to 10 MHz, ± 0.1% accuracy, Single Pulse function	Tektronix FG 5010	Checking minimum pulse width
3. Counter-Timer	Resolution to 1 ppm	Tektronix DC 5010	Checking Time Tag Clock
4. Calibrator/Generator	Variable DC Voltage to ± 50 V DC, accuracy to 0.01%	Data Precision 8200 Calibrator	Checking DC Volts accuracy
5. DD50S interconnect assembly	DD-50S (female) connector, Tektronix part number 131-1344-00, prototype bus wire	Assemble as shown in Figure A–1	Interconnecting electrical signals
6. Coaxial BNC Cable (two)	50 Ω, 36 in., male to male BNC connectors	Tektronix part number 012-0482-00	Interconnecting electrical signals
7. Connector, BNC T	50 Ω , BNC female to BNC female to BNC male	Tektronix part number 103-0030-00	Interconnecting electrical signals

Table A–1: Required Test Equipment (Cont.)

Item Number and Description	Minimum Requirements	Example	Purpose
8. Adapter, BNC femal to Clip Leads	50 Ω, BNC female to dual Clip Leads	Tektronix part number 013-0076-00	Interconnecting electrical signals
9. Adapter, BNC male to Probe Tip	50 Ω, BNC male to oscilloscope probe	Tektronix part number 013-0195-00	Interconnecting electrical signals
10. Adapter, BNC female to dual banana	50 Ω, BNC female to dual banana	Tektronix part number 013-0090-00	Interconnecting electrical signals

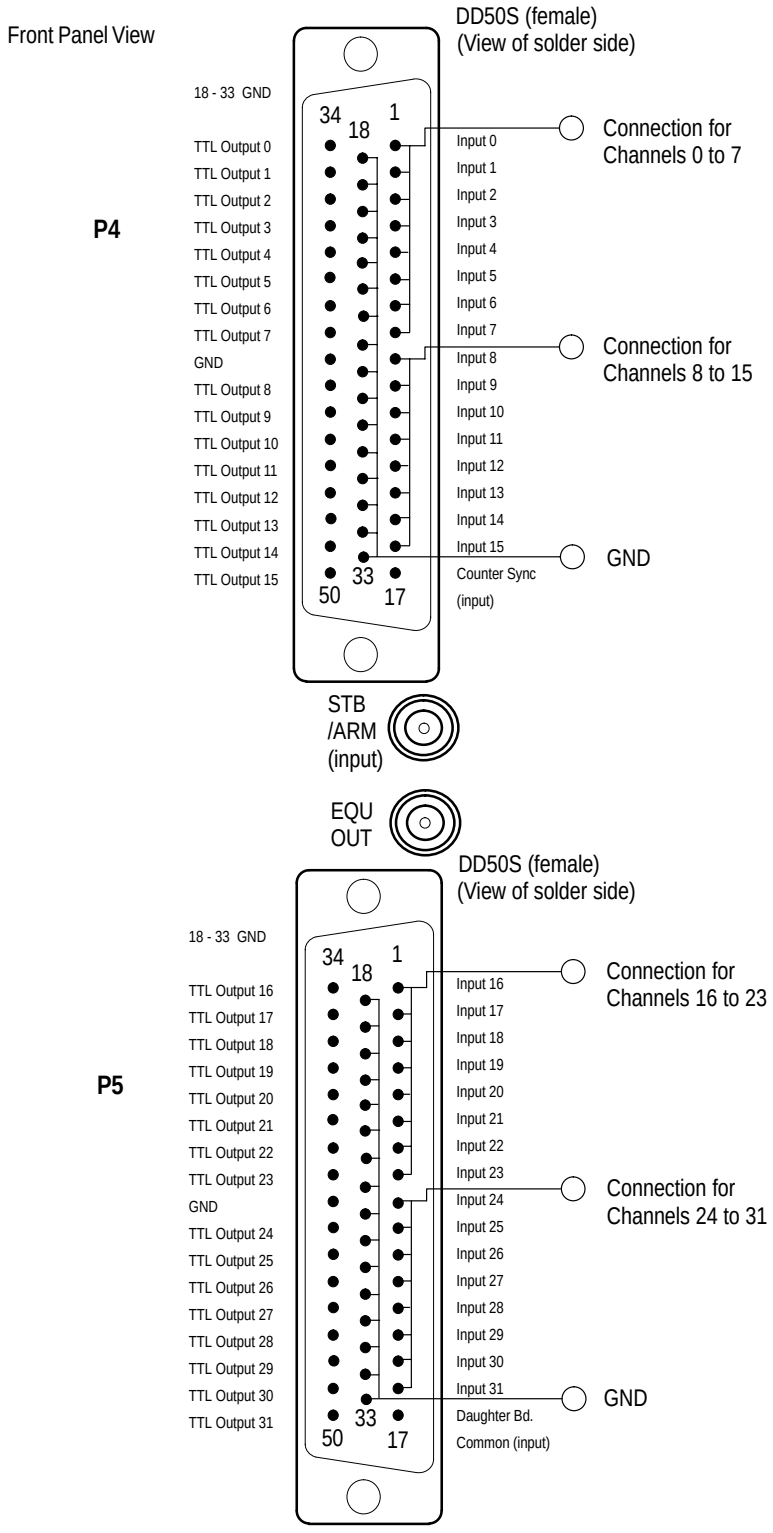


Figure A–1: DD-50S Interconnect Assembly

VX4286 Under-Test Configuration

The VX4286 under-test must be installed in an approved VXIbus system. At a minimum, the system must contain the elements listed in Table A–2.

Table A–2: Elements of a Minimum VX4286 Under-Test System

Item Number and Description	Minimum Requirements	Example	Purpose
1. VXIbus Mainframe	One available slot (in addition to the Slot 0 Resource Manager) for the VX4286 under-test	Tektronix VX1410 IntelliFrame	Provides power, cooling, and backplane for VXIbus modules
2. Slot 0 Resource Manager	Resource Mgr., Slot 0 Functions, IEEE 488 GPIB Interface	VX4521 Slot 0 Resource Mgr.	Provides Slot 0 Resource Mgr. functions, and GPIB interface
3. VXIbus System Controller	VXIbus-Talker/Listener/Controller	486 PC with National GPIB PC2A & NI-488.2M software, GPIB cable	Provides VXIbus command and response interface

Test System Configuration

Table A–3 describes the VXIbus system configuration assumed in this procedure. If your configuration is different, please note that you will observe your device names and addresses in test sequences. No secondary addressing is assumed.

Table A–3: Test System Configuration Assumed

Device	GPIB Device Name	VXI Slot	VXIbus Logical Address	GPIB Primary Address
GPIB0	GPIB0	(PC card)	NA	30
VX4521	VX4521	Slot 0	0D (hex)	13
VX4286 under-test	VX4286	Slot 1	01	1

Test Record

Photocopy the Test Record which follows to record your results.

Table A–4: VX4286 Test Record

VX4286 Serial Number:	Temperature and Relative Humidity:
Date of Last Calibration:	Verification Performed by:
Certificate Number:	Date of Verification:

VXIbus Interface	**Logical Address, IEEE Address, Slot No., MFG., Model, etc.**	
System Configuration Response		
Extended Self Test Verification (S1)	**Passed**	**Failed**

Acquisition		**Passed**	**Failed**
STB/ARM input			
VXIbus Request True interrupt			
EQU OUT signal			
Minimum Pulse Width & TTL Output	Inputs 0 to 7		
	Inputs 8 to 15		
	Inputs 16 to 23		
	Inputs 24 to 31		

DC Voltage Accuracy ±50 Volt (Limits)		**AVE** 49.945 to 50.055	**MIN** 49.895 to 50.030	**MAX** 49.970 to 50.105		**AVE** –50.055 –49.945	**MIN** –50.105 –49.970	**MAX** –50.030 –49.895
	Input 0							
	Input 1							
	Input 2							
	Input 3							
	Input 4							
	Input 5							
	Input 6							
	Input 7							
	Input 8							
	Input 9							
	Input 10							
	Input 11							
	Input 12							

Table A–4: VX4286 Test Record (Cont.)

DC Voltage Accuracy ±50 Volt (Limits)		AVE 49.945 to 50.055	MIN 49.895 to 50.030	MAX 49.970 to 50.105		AVE –50.055 –49.945	MIN –50.105 –49.970	MAX –50.030 –49.895
	Input 13							
	Input 14							
	Input 15							
	Input 16							
	Input 17							
	Input 18							
	Input 19							
	Input 20							
	Input 21							
	Input 22							
	Input 23							
	Input 24							
	Input 25							
	Input 26							
	Input 27							
	Input 28							
	Input 29							
	Input 30							
	Input 31							

DC Voltage Accuracy ±10 Volt (Limits)		AVE 9.985 to 10.015	MIN 9.980 to 10.010	MAX 9.990 to 10.020		AVE –10.015 –9.985	MIN –10.020 –9.990	MAX –10.010 –9.980
	Input 0							
	Input 1							
	Input 2							
	Input 3							
	Input 4							
	Input 5							
	Input 6							
	Input 7							

Table A–4: VX4286 Test Record (Cont.)

DC Voltage Accuracy ±10 Volt (Limits)		AVE 9.985 to 10.015	MIN 9.980 to 10.010	MAX 9.990 to 10.020		AVE –10.015 –9.985	MIN –10.020 –9.990	MAX –10.010 –9.980
	Input 8							
	Input 9							
	Input 10							
	Input 11							
	Input 12							
	Input 13							
	Input 14							
	Input 15							
	Input 16							
	Input 17							
	Input 18							
	Input 19							
	Input 20							
	Input 21							
	Input 22							
	Input 23							
	Input 24							
	Input 25							
	Input 26							
	Input 27							
	Input 28							
	Input 29							
	Input 30							
	Input 31							

Self Test

The VX4286 includes a built-in self test function (BITE) which runs automatically each time the power is turned on and when the internal self-test (IST) is executed.

BITE uses internal routines and reference circuitry which verifies all input thresholds to within 5% of their required accuracy. It also verifies the integrity of on–board RAM, NVRAM, processor, and custom gate arrays.

In addition to BITE, the front panel indicator lights display the current status of module power, self test results, and the assertion of SYSFAIL*. If the module loses any of its power voltages, the Failed light will be on, the Power light will be off, and SYSFAIL* will be asserted. Following a successful VXIbus system startup sequence, the green PWR light on the VX4286 front panel indicates that the self test has passed and that all power supplies are operational.

***NOTE**. If you experience an error indication from the VX4286-under-test, or any other VXIbus module, investigate and correct the problem before proceeding. Common items to check are logical address conflicts (primary and secondary; see Table A–3), breaks in the VXIbus daisy chain signals, improper seating of a module, loose GPIB cable, or loose or blown fuses.*

Performance Verification Tests

This Performance Verification procedure may be executed in any order. You may use any VXI system which meets the requirements in Table A–2, however the test sequences are structured for a system configuration as described in Table A–3.

***NOTE**. If at any time you do not observe the expected result, check the front panel ERROR light. If it is on, perform Err? queries until you receive a response of "00, NO ADDITIONAL ERRORS TO REPORT..". The front panel ERROR light should then be off. To quickly clear all errors, send an "rst" (reset) command.*

VXIbus Interface

This sequence verifies that the VX4286 configures correctly and communicates properly with the system controller. It assumes a VXI system configuration as specified in Table A–3, and in particular, utilizes the VX4521 Resource Manager "table" command for verifying the system configuration. If your VXI system uses a different Resource Manager, you must substitute commands specific to that Resource Manager-Controller to verify your system configuration.

Equipment Requirements	No test equipment required.
Prerequisites	All prerequisites listed on Page A–22

***NOTE**. If you are using National Instruments NI-488.2 software you may wish to select the* `buffer 1` *display mode to allow more comfortable viewing of the ASCII response. To do so, type* `buffer 1` *as directed in Table A–5.*

1. If using the VX4521 Slot 0 Resource Manager, send the TABLE command to verify the system configuration. If using a different Controller, perform the equivalent function to confirm the responses shown in Table A–5.

Table A–5: VXIbus System Configuration

Command to Type	Response to Verify
`ibic`	
`buffer 1`	(Invokes National Instruments "ASCII only buffer display")
`ibfind VX4521`	(Address Resource Manager)
`ibwrt "table"`	(Solicit VXI system information and module identification)

`3*ibrd 100`	02.. (Indicates that two modules are in this system.)
	
	`LA 0, IEEE 13, Slot 0, MFG FFDh, MODEL VX4521, PASS, , RM..`
	
	`LA 1, IEEE 01, Slot 1, MFG FFCh, MODEL VX4286, PASS TRIGGER;LOCK;READ STB, MESG, 0, V1.3, NORMAL ..`

2. Send the self-test command to ensure module communication and general functionality. Following the command, verify that the front panel ERROR light is off and that there are no error responses queued up.

`ibfind VX4286`

`ibwrt "ist"`

`ibrd 100` (Observe a "00,NO ADDITIONAL ERRORS TO REPORT..)

STB/ARM Input, VXIbus Interrupt, EQU OUT Out, Minimum Data Pulse Width, TTL Output

This sequence verifies the STB/ARM input (arms the module to begin monitoring the inputs), the generation of a VXIbus Request True interrupt, the EQU OUT pulse, the ability of the VX4286 to recognize an input data pulse of at least 3 µs duration and 150 mV in amplitude, and the generation of a corresponding TTL Output data pulse.

Equipment Requirements	Digital Oscilloscope (item 1) Function Generator (item 2) BNC T Adapter (item 7) BNC female to Clip Lead Adapter (item 8) BNC to Probe Tip Adapter (item 9) Coaxial Cable, two (item 6) DD50S Interconnect Adapter (item 5)
Prerequisites	All prerequisites listed on page A–22

1. Attach the DD50S interconnect Adapter to the VX4286 P4 connector.
2. Attach a BNC-T connector to the function generator Output. Attach one end of a coaxial cable to one side of the BNC-T and attach a BNC-to-Clip Lead Adapter to the opposite end of the coaxial cable. Connect the red Clip Lead to the 0-to-7 inputs of the VX4286, and the black Clip Lead to the DD50S common GND (see Figure A–1).
3. Using a second coaxial cable, connect the other side of the BNC-T to the VX4286 STB/ARM input.
4. Set the function generator for a square wave with a frequency of 167 kHz, an amplitude of 2.0 V_{pp}, and an offset of +1.0 V. Select Burst mode and set the number of bursts to one. Enable the output.
5. Connect the channel 1 of the oscilloscope to the VX4286 0-to-7 inputs. Attach the ground clip to the common ground bus of the DD50S interconnect Adapter. Connect channel 2 to the EQU OUT using a probe tip-to-BNC Adapter (See Figure A–1). Configure the oscilloscope as follow:
   - **a.** Set both channel 1 and channel 2 to 1.00 V/division and 20 MHz bandwidth.
   - **b.** Set the horizontal to 100 µs/division.
   - **c.** Position the channel 1 zero reference trace to the center horizontal graticule and the channel 2 trace to the first horizontal graticule above the bottom of the display.
   - **d.** Set the trigger source to channel 1, the trigger level to one horizontal graticule above the center of the display (i.e. to trigger on a 1.0V signal level from channel 1), and reset the mode to Normal.

6. Using the following commands, set the VX4286 to the power–on default state, to have a trigger equation which will capture signals on Inputs 0-to-7, to assert a VXIbus Request True interrupt on EQU true, to be armed by a positive pulse received on the front panel STB/ARM connector, to un-tristate the TTL outputs, and to request data (and reenable channels) from the Event Buffer. (Note: The power-on default threshold level for Inputs 0-to-31 and STB/ARM is 1.4V. Also, the EQU command specifies which channels are to be enabled for collection in the Event buffer, in this case 0-to-7, and enables the front panel EQU OUT signal to pulse concurrent with data capture.)

```
set VX4286

ibwrt "rst;equ 0to7;int 1;arm +8;output on;data? r"
```

7. Check that the front panel ARM light is not on. Also, perform a serial poll with the VX4286 and verify that there is no VXIbus Request True event pending.

`ibrsp` (Observe: Poll: 0x0 (decimal:0))

8. Press the force manual trigger button to clear the oscilloscope display. Press the manual trigger button on the function generator and verify that the ARM light is now on.

9. Press the manual trigger a second time and verify the function generator input pulse on channel 1 of the oscilloscope (approximately 3 µs) and the corresponding negative EQU OUT pulse on channel 2 (approximately 2.4µs). The EQU OUT pulse occurs about 200 µs after the function generator input pulse.

10. Perform a serial poll with the VX4286 and verify that a VXIbus Request True event is pending (an S displayed in the second display digit of the VX4521).

`ibrsp` (Observe Poll: 0x41 (decimal:65))

11. Perform two Event Buffer queries and observe the Time Tag and Channel Data followed by “NO ENTRIES”.

(Example Response: 79.7384: +00,+01,+02,+03,+04,+05,+06,+07 ..)

`ibrd 100` (Observe: [TIME TAG]: [CHANNEL DATA])

`ibrd 100` (Observe: “NO ENTRIES..”)

(Following the read query, the VX4286 will be rearmed and will once again capture a manually triggered pulse from the function generator.)

12. Remove the coaxial cable connecting the STB/ARM input to the function generator (disconnect both ends of this cable and set aside). Reset the

function generator Amplitude to 150 mV_{pp} with an offset of 75 mV (display will round off to 0.08).

13. Move the channel 2 oscilloscope probe from the EQU OUT connector to the TTL Output 0 signal of the VX4286 (see Figure A–1).

14. Set channel 1 of the oscilloscope to 100 mV/division and the horizontal to 20 µs/division. Reset the trigger source to channel 2 and the trigger level to the 2nd graticule from the bottom of the display.

15. Reset the VX4286 to the power-on default state, to trigger on a 100 mV input level, with a capture equation specified to acquire "threshold crossing signals" on Inputs 0-to-7, to be permanently armed, to un-tristate the TTL outputs, and to return data from the Event Buffer when queried (reenabling channels following query).

```
ibwrt "rst;trg0to31>0.1;equ0to7;arm on;output on;data?r"
```

16. Press the force manual trigger button to clear the oscilloscope, then press the manual trigger button on the function generator. Verify the TTL Output pulse on channel 2 of the oscilloscope (approximately 100 µs) concurrent with the input pulse on channel 1 (approximately 3µs).

17. Query the Event buffer and and verify the Time Tag and Channel Data. (Note: The VX4286 display will flash CH00 at the same time an input pulse is recognized.)

`ibrd 100` (Observe: [TIME TAG]: [CHANNEL DATA])

18. To verify Minimum Pulse capture and the TTL Outputs for the remaining (1-to-7) channels, move the channel 2 oscilloscope probe, to the next TTL Output channel and repeat steps 16 and 17.

19. To verify Minimum Pulse capture and the TTL Outputs for channels 8-to-15:

a. Move the red signal generator Clip Lead and the channel 1 oscilloscope probe to the inputs for channels 8-to-15 (see Figure A–1).

b. Reset the VX4286 capture equation to acquire threshold crossing signals on Inputs 8-to-15.

```
ibwrt "equ 8to15"
```

c. Move the channel 2 oscilloscope probe to the TTL Output channel you wish to verify (8-to-15) and repeat the command sequence illustrated in steps 16 and 17.

20. To verify the Minimum Pulse capture and TTL Outputs for channels 16-to-23:

a. Move the DD50S interconnect Adapter from the P4 to P5 connector.

b. Move the red signal generator Clip Lead and the channel 1 oscilloscope probe to the VX4286 inputs for channels 16-to-23 (Figure A–1).

c. Reset the VX4286 capture equation to acquire threshold crossing signals on Inputs 16-to-23

```
ibwrt "equ 16to23"
```

d. Move the channel 2 oscilloscope probe to the TTL Output channel you wish to verify (16-to-23) and repeat the command sequence illustrated in steps 16 and 17.

21. To verify the minimum pulse capture and TTL Outputs for channels 24-to-31:

a. Move the red signal generator Clip Lead and the channel 1 oscilloscope probe to inputs for channels 24-to-31 (Figure A–1).

b. Reset the capture equation to acquire threshold crossing signals on Inputs 24-to-31.

c. Move the channel 2 oscilloscope probe, in-turn, to the TTL Output channel you wish to verify (24-to-31) and repeat the command sequence illustrated in steps 16 and 17.

```
ibwrt "equ 24to31"
```

DC Voltage Accuracy

This sequence verifies the accuracy of the volt meter read back feature for the ± 50V and ± 10V ranges.

Equipment Requirements	DC Voltage Calibrator (item 4) BNC Coaxial Cable, one (item 6) BNC female to Clip Lead Adapter (item 8) BNC Dual Banana Connector (item 10)
Prerequisites	All prerequisites listed on page A–22

1. Attach the DD-50S Interconnect Assembly to P4 as shown in Figure A–1.

2. Connect the Voltage Calibrator to input channels 0-to-7 of the VX4286 using a Dual-Banana connector a Coaxial cable, and a BNC to Clip Lead adapter.

3. Set the Calibrator to +50.0V DC.

4. Use the following commands to set the VX4286 to the power–on default state, for a voltage measurement on all channels specified (0-to-7 in this first pass; 8-to-15, 16-to-23, 24-to-31 on subsequent passes), to use the high voltage range, and to report the results using labels.

`set VX4286`

`ibwrt "rst;vaH? L,0to7"` (8-15, 16-23, 24-31 on later passes)

5. Perform eight successive acquisitions and verify the responses relative to the limits shown in the Test Record. (For controllers that do not support successive read back, the VOLTNEXT? command can be sent between readings.)

   `8*ibrd 100` (Verify responses relative to the Test Record.)

6. Set the Calibrator to –50.0 V DC.

7. Reacquire and verify the response to the limits shown in the Test Record.

   `ibwrt "vaH? L,0to7"` (use 8-15, 16-23, 24-31 on other passes)

   `8*ibrd 100` (Verify responses relative to the Test Record.)

8. Set the Calibrator to +10.0 V DC.

9. Reset the VX4286 for a voltage measurement on all channels specified, using the low voltage range and verify the responses relative to the Test Record.

   `ibwrt "vaL? L,0to7"` (8-15, 16-23, 24-31 on later passes)

   `8*ibrd 100` (Verify responses relative to the Test Record.)

10. Set the Calibrator to –10.0 V DC.

11. Reacquire and verify the response to the limits shown in the Test Record.

    `ibwrt "vaL? L,0to7"` (8-15, 16-23, 24-31 on later passes)

    `8*ibrd 100` (Verify responses relative to the Test Record.)

12. Connect the Voltage Calibrator to input channels 8-to-15 of the VX4286 (as shown in Figure A–1) then repeat steps 3 to 11, substituting channel designation `8to15` in place of `0to7`.

13. Move the DD50S Interconnect Adapter from the VX4286 P4 connector to the P5 connector. Connect the Voltage Calibrator to input channels 16 through 23 (as shown in Figure A–1) then repeat steps 3 to 11, substituting channel designation `16to23` in place of `0to7`.

14. Connect the Voltage Calibrator to input channels 24-to-31 then repeat steps 3 to 11, substituting channel designation `23to31` in place of `0to7`.

Time Tag Clock Accuracy

This sequence verifies the accuracy of the 500 kHz Time Tag clock to be within 50 ppm for the standard VX4286 module or for 5 ppm for Option-1.

Equipment Requirements	Frequency Counter (item 3) BNC Coaxial Cable, one (item 6) BNC T Adapter (item 7) BNC to Probe Tip Adapter (item 9)
Prerequisites	All prerequisites listed on page A–22

1. Attach a BNC-T Adapter to the VX4286 front panel EQU OUT connector.
2. Connect the frequency counter to one side of the BNC-T with a coaxial cable. Attach the BNC to Probe Tip Adapter to the other side of the BNC-T and insert the oscilloscope probe.
3. Reset the VX4286 to the power-on state, to enable the TTL Outputs, to assert the 500 kHz Time Tag signal on the EQU OUT connector and on TTL Outputs 15 and 31. Verify the Time Tag frequency of 500 kHz ± 25 Hz on the frequency counter and on the oscilloscope (approximately 3.5 V amplitude).

   ```
   set VX4286

   ibwrt "rst;output on;fcal s" (Observe 500 kHz ± 25 Hz)
   ```

4. Using the oscilloscope probe, verify a 500 kHz TTL signal on TTL Output 15 (P4) and TTL Output 31 (P5).

This completes the VX4286 verification procedure.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Appendix G
User Service

This appendix contains service-related information that covers the following topics:

- Preventive maintenance
- User-replaceable Parts

Preventive Maintenance

You should perform inspection and cleaning as preventive maintenance. Preventive maintenance, when done regularly, may prevent malfunction and enhance reliability. Inspect and clean the module as often as conditions require by following these steps:

1. Turn off power and remove the module from the VXIbus mainframe.
2. Remove loose dust on the outside of the instrument with a lint-free cloth.
3. Remove any remaining dirt with lint-free cloth dampened in a general purpose detergent-and-water solution. Do not use abrasive cleaners.

User-Replaceable Parts

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable.

User-Replaceable Parts

Part Description	Part Number
User Manual	070-9143-XX
Label, Tek CDS	950-0663-00
Label, VXI	950-1485-00
Fuse, **Littelfuse 2 Amp 125 V Fast**	159-0128-00
Fuse, **Littelfuse 4 Amp 125 V Fast**	159-0374-00
Collar Screw, Metric 2.5 × 11 Slotted	950-0952-00
Shield, Front	950-1320-00
Screw, Phillips Metric 2.5 × 4 FLHD SS	211-0867-00

Appendix H
Adjustment and Calibration

The VX4286 Module module must be calibrated every twelve months for the module to meet its published accuracy specifications. Calibrate the VX4786 Module at the temperature at which it will be operating. Calibration to the published accuracy specifications has been performed at Tektronix Inc. prior to shipping. Allow a ten minute warm-up period before performing the calibration.

Test Equipment Required

- 73A-853 Extender Card or equivalent
- Voltage calibrator with a 50V DC range absolute accuracy of 0.03%, and maximum noise specification of < 1 mV rms (DC to 10 KHz).

Additional test equipment required with Option 01 installed:

- 1 MHz frequency standard
- Dual trace 10 MHz or greater oscilloscope
- Standard screwdriver with 0.1" blade or 1/16" square end adjustment tool

Calibration Procedure

Voltage Threshold Calibration For Standard VX4286:

Allow a ten minute warm-up period before performing the calibration.

1) Repeat steps 2 through 14 below until all channels have been calibrated.

2) Use the CAL S,[N]<LF> command to initiate the calibration procedure for a single channel [N]. For example, for the first channel, CAL S,0<LF> would be sent. To speed up the process, a number of channels can be calibrated at once, depending upon the output current capability of the calibrator. For instance, if the calibrator is capable of outputting 8 mA, up to eight channels could be calibrated at the same time. (8 mA * 52K ohms min input impedance / 50 volts = 8.3 channels). In this case, the first channels would be programmed with CAL S,0 TO 7<LF>, the next with CAL S,8 TO 15<LF>, and so forth.

3) Connect the output of the calibrator to the channel inputs of all channels given in the CAL S command sent in step 2. Do not connect the calibrator to any other inputs, as this could violate the calibrator specification for maximum output current.

   An exception is when eight channels are being calibrated at once and they are one of the groups 0-7, 8-15, 16-23, or 24-31. In this case, the VX4286 Module will relay-isolate the unused channels upon reception of the CAL S command. The isolated channels would be 8-15 for calibrating channels 0-7, 0-7 for 8-15, 24-31 for 16-23 and 16-23 for 31-24. This isolation allows calibrators with enough output current for eight channels but not for sixteen channels to be directly connected to all sixteen channels on the connector. The isolated channels will be reconnected with the next CAL E, CAL AB, CAL S, or RST command.

4) Program the calibrator for -10.000 volts.

5) Send the CAL A,-10 command to the VX4286. The CAL A command will automatically wait five millilseconds before beginning the calibration, to accommodate the settling time of the calibrator. If the settling time of the calibrator is greater than five milliseconds, be sure that enough settling time has passed between the setting of the calibrator and the programming of the VX4286 module.

6) Wait for the CAL A command to complete, a period of a half-second times the number of channels specified with the CAL S command.

7) Read the VX4286. If the 00,NO ADDITIONAL ERRORS TO REPORT response is returned, continue to next step. If the 62,CAL ERROR CHAN [CHAN]: [VOLT] VOLTAGE READS TOO LOW/HIGH response is returned, where [CHAN] is the channel number, and [VOLT] is -10, then verify that the calibrator is putting out the correct voltage within its specified accuracy.

8) Repeat steps 4 through 7 three more times using voltages +10, -50, and +50 where -10 volts was previously used.

9) Send the CAL E command to the VX4286.

10) Read the response of the VX4286. If the response reads 64,CALIBRATION COMPLETE, calibration was successful for these channel(s).

    If the response read was not 64,CALIBRATION COMPLETE, calibration was unsuccessful, and the previous calibration values remain unchanged. If the error is 63,CAL ERROR: ALL VOLTAGES NOT RECEIVED, this indicates that a successful CAL A command was not received for each voltage.

11) Program the calibrator for -10.000 volts.

12) Send a VOLTALL?L,[N]<LF> command, where [N] specifies the same channels as in step 2.

13) Read the response from the VX4286. There is one message per channel. For controllers that do not support successive readbacks, the VOLTNEXT? command can be sent between readings (see the example below).

Verify that the voltages returned are as follows:

	Average	Minimum	Maximum
+10V	9.985 to 10.015	9.980 to 10.010	9.990 to 10.020
-10V	-10.015 to -9.985	-10.020 to -9.990	-10.010 to -9.980
+50V	49.945 to 50.055	49.895 to 50.030	49.970 to 50.105
-50V	-50.055 to -49.945	-50.105 to -49.970	-50.030 to -49.895

If the voltages returned are outside these limits, make sure that excess noise does not exist on the calibration output. If this is not the problem, consult Tektronix/CDS at 1-800-CDS-ATE1.

14) Repeat steps 11 through 13 three more times using voltages of +10, -50, and +50 where -10 volts was previously used.

15) Repeat the procedure again, continuing from step 2, until all channels have been calibrated.

Note that this procedure is the suggested order. The voltages may be applied in any order.

Typical Calibration

The responses from the VX4286 are shown underlined. (Note that the VOLTNEXT? command is not required unless successive readback is not supported.)

```
CAL S,0TO7<LF>
CAL A,-10<LF>
(4 second delay)
00,NO ADDITIONAL ERRORS TO REPORT<CR><LF>
CAL A,10<LF>
(4 second delay)
00,NO ADDITIONAL ERRORS TO REPORT<CR><LF>
CAL A,-50<LF>
(4 second delay)
00,NO ADDITIONAL ERRORS TO REPORT<CR><LF>
CAL A,50<LF>
(4 second delay)
00,NO ADDITIONAL ERRORS TO REPORT<CR><LF>
VOLTALL? L,0TO7<LF>
AVE =  -9.998, MIN =  -9.998, MAX =  -9.998<CR><LF>
```

```
VOLTNEXT?<LF>
AVE = -10.000, MIN = -10.000, MAX = -10.000<CR><LF>
VOLTNEXT?<LF>
AVE = -10.004, MIN = -10.006, MAX = -10.002<CR><LF>
VOLTNEXT?<LF>
AVE =  -9.998, MIN =  -9.998, MAX =  -9.998<CR><LF>
VOLTNEXT?<LF>
AVE = -10.000, MIN = -10.000, MAX = -10.000<CR><LF>
VOLTNEXT?<LF>
AVE = -10.004, MIN = -10.006, MAX = -10.002<CR><LF>
VOLTNEXT?<LF>
AVE =  -9.998, MIN =  -9.998, MAX =  -9.998<CR><LF>
VOLTNEXT?<LF>
AVE = -10.000, MIN = -10.000, MAX = -10.000<CR><LF>
VOLTALL? L,0TO7<LF>
AVE =   9.998, MIN =   9.998, MAX =   9.998<CR><LF>
AVE =  10.000, MIN =  10.000, MAX =  10.000<CR><LF>
AVE =  10.004, MIN =  10.002, MAX =  10.006<CR><LF>
AVE =   9.998, MIN =   9.998, MAX =   9.998<CR><LF>
AVE =  10.000, MIN =  10.000, MAX =  10.000<CR><LF>
AVE =  10.004, MIN =  10.002, MAX =  10.006<CR><LF>
AVE =   9.998, MIN =   9.998, MAX =   9.998<CR><LF>
AVE =  10.000, MIN =  10.000, MAX =  10.000<CR><LF>
VOLTALL? L,0TO7<LF>
AVE = -49.987, MIN = -50.000, MAX = -49.975<CR><LF>
AVE = -50.000  MIN = -50.000, MAX = -50.000<CR><LF>
AVE = -50.013, MIN = -50.025, MAX = -50.000<CR><LF>
AVE = -49.987, MIN = -50.000, MAX = -49.975<CR><LF>
AVE = -50.000  MIN = -50.000, MAX = -50.000<CR><LF>
AVE = -50.013, MIN = -50.025, MAX = -50.000<CR><LF>
AVE = -49.987, MIN = -50.000, MAX = -49.975<CR><LF>
AVE = -50.000  MIN = -50.000, MAX = -50.000<CR><LF>
VOLTALL? L,0TO7<LF>
AVE =  49.987, MIN =  49.975, MAX =  50.000<CR><LF>
AVE =  50.000  MIN =  50.000, MAX =  50.000<CR><LF>
AVE =  50.013, MIN =  50.000, MAX =  50.025<CR><LF>
AVE =  49.987, MIN =  49.975, MAX =  50.000<CR><LF>
AVE =  50.000  MIN =  50.000, MAX =  50.000<CR><LF>
AVE =  50.013, MIN =  50.000, MAX =  50.025<CR><LF>
AVE =  49.987, MIN =  49.975, MAX =  50.000<CR><LF>
AVE =  50.000  MIN =  50.000, MAX =  50.000<CR><LF>
CAL S,8TO15<LF>
...
CAL S,16TO23<LF>
...
CAL S,24TO31<LF>
...
```

Frequency Calibration For VX4286 with Option 01 Installed:

Allow a ten minute warm-up period before performing the calibration.

1) Use the FCAL S command to initiate the frequency calibration procedure.

2) Send an OUTPUT ON command (this command is required only if a Channel 15 or 31's TTL Output is being used in the next step).

3) Connect channel 1 of the oscilloscope to the EQU OUT BNC connector of the VX4286. The signal on the EQU OUT connector can also be accessed on the channel 15 TTL Output (P4) or channel 31's TTL Output (P5).

4) Connect channel 2 of the oscilloscope to a 1 MHz frequency source. The scope should be triggered to this channel, and a stable 1 MHz signal should be displayed on the oscilloscope.

5) Use a screwdriver or adjustment tool to adjust the crystal oscillator until the horizontal rolling of channel 1 with respect to the stable channel 2 is minimized. The adjustment location is shown in Figure 1. The rolling should be brought down to a level where channel 1 rolls less than a horizontal distance of 1 µsec in a 5 second period (1 µsec is one period of the 1 MHz frequency).